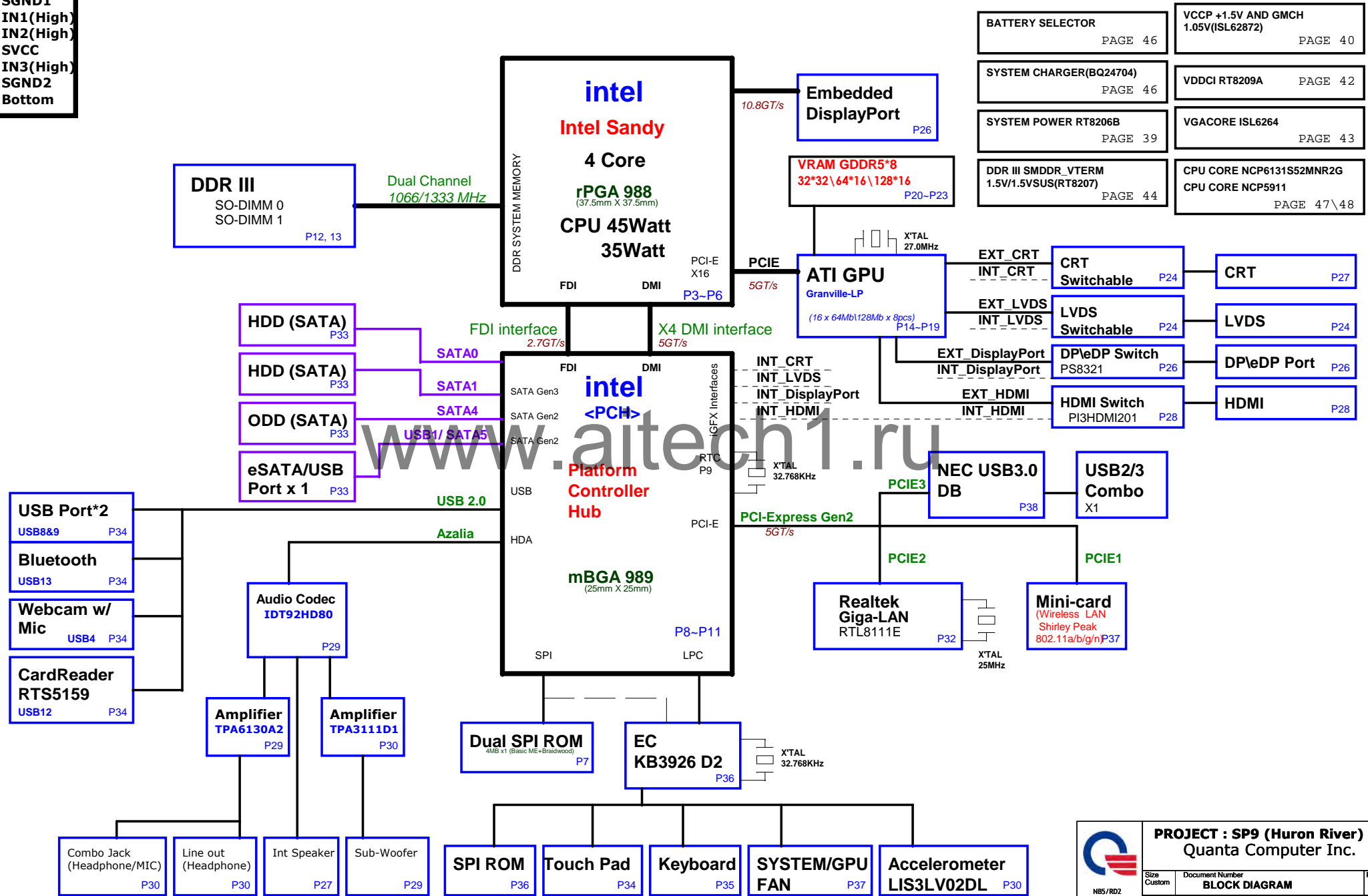
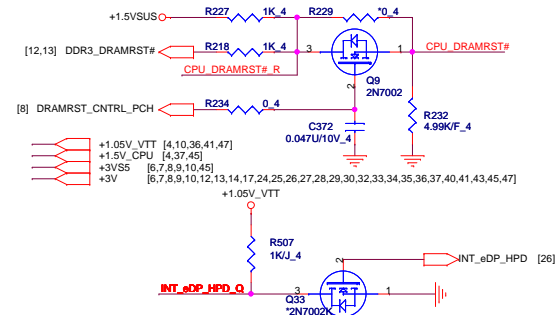


LAYER 1 : TOP
 LAYER 2 : SGND1
 LAYER 3 : IN1(High)
 LAYER 4 : IN2(High)
 LAYER 5 : SVCC
 LAYER 6 : IN3(High)
 LAYER 7 : SGND2
 LAYER 8 : Bottom

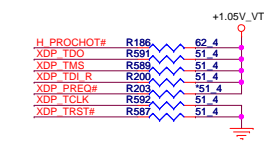
SP9 BLOCK DIAGRAM

01





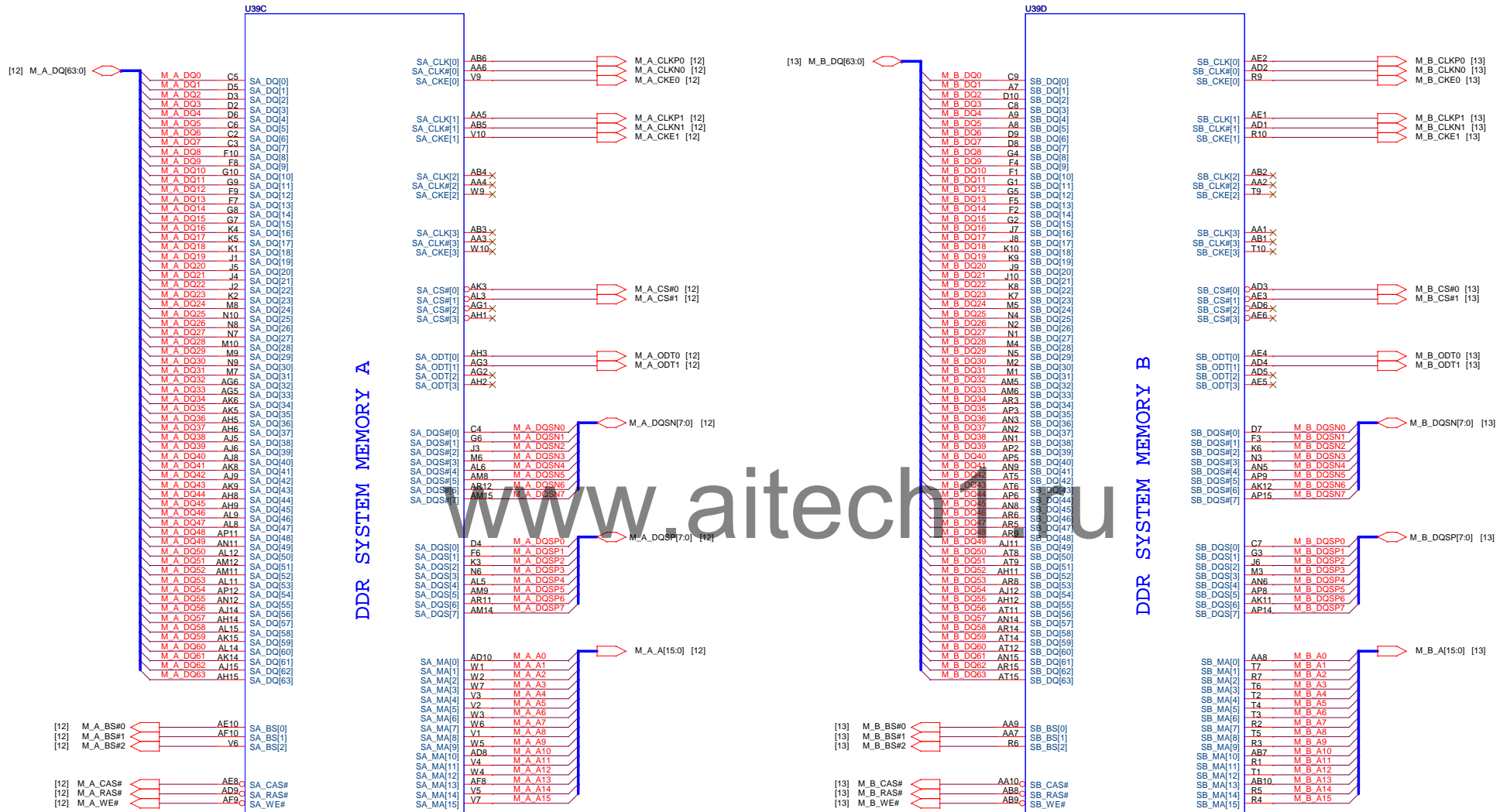
Processor pull-up (CPU)



NB5/RD2

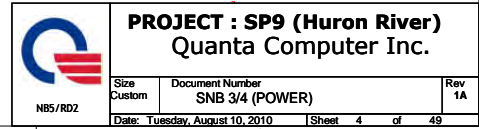
Size Custom	Document Number SNB 1/4 (PCIE&DMI&FDI)	Rev 1A
Date: Tuesday, August 10, 2010		Sheet 2 of 49

Sandy Bridge Processor (DDR3)

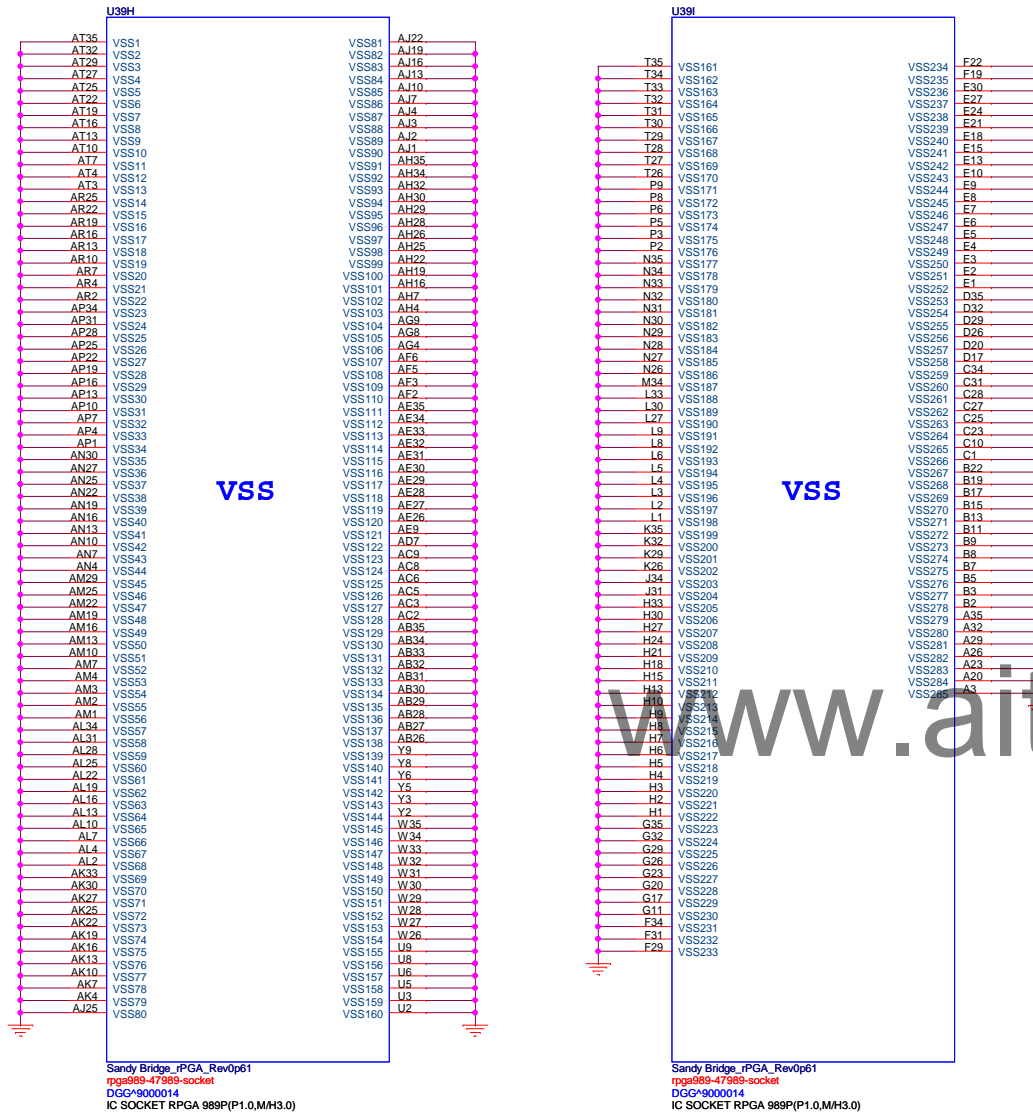


Sandy Bridge_rPGA_Rev0p61
 rpg989-47989-socket
 DGG-9000014
 IC SOCKET RPGA 989P(P1.0,M/H3.0)

Sandy Bridge_rPGA_Rev0p61
 rpg989-47989-socket
 DGG-9000014
 IC SOCKET RPGA 989P(P1.0,M/H3.0)



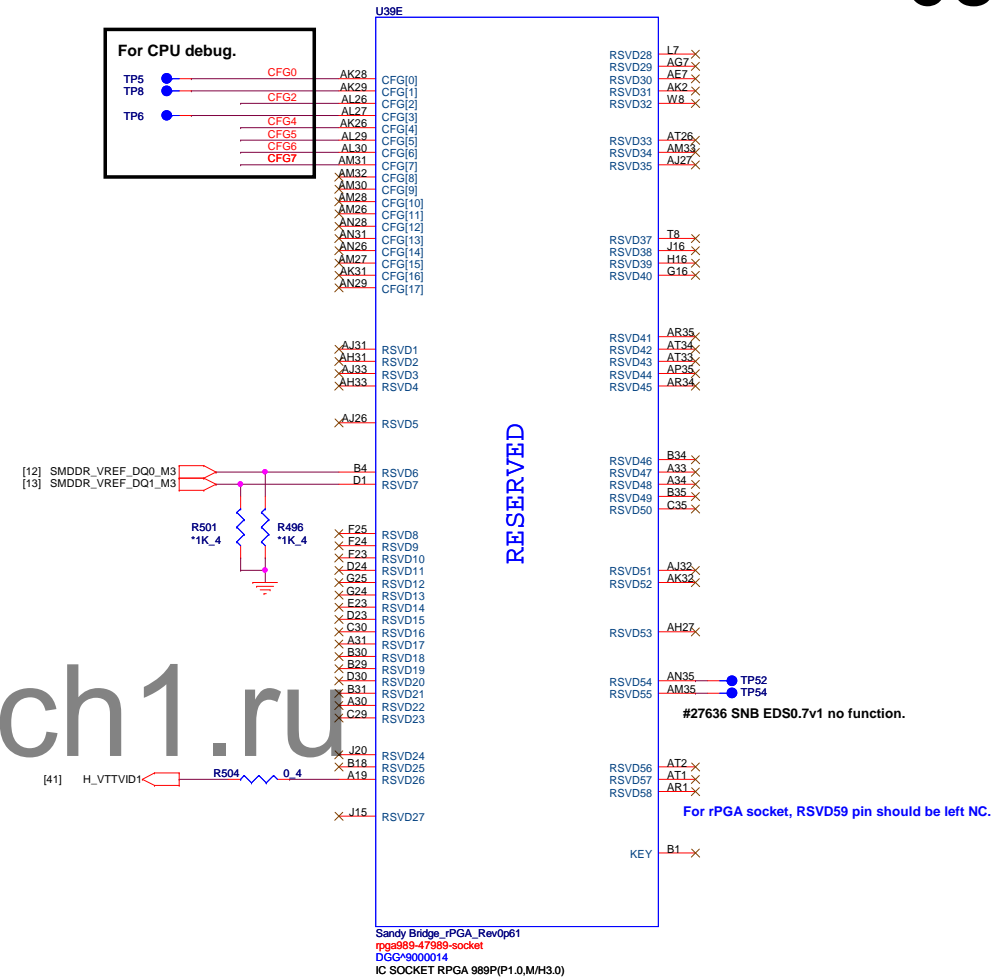
Sandy Bridge Processor (GND)



Sandy Bridge_rPGA_Rev0p61
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DGG*9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

Sandy Bridge_rPGA_Rev0p61
rpg989-47989-socket
DGG*9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

Sandy Bridge Processor (RESERVED, CFG)



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DGG*9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

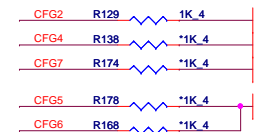
Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

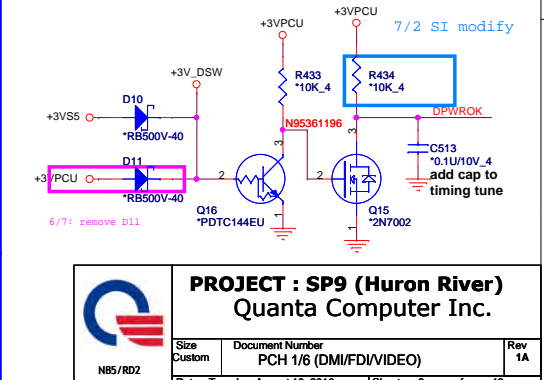
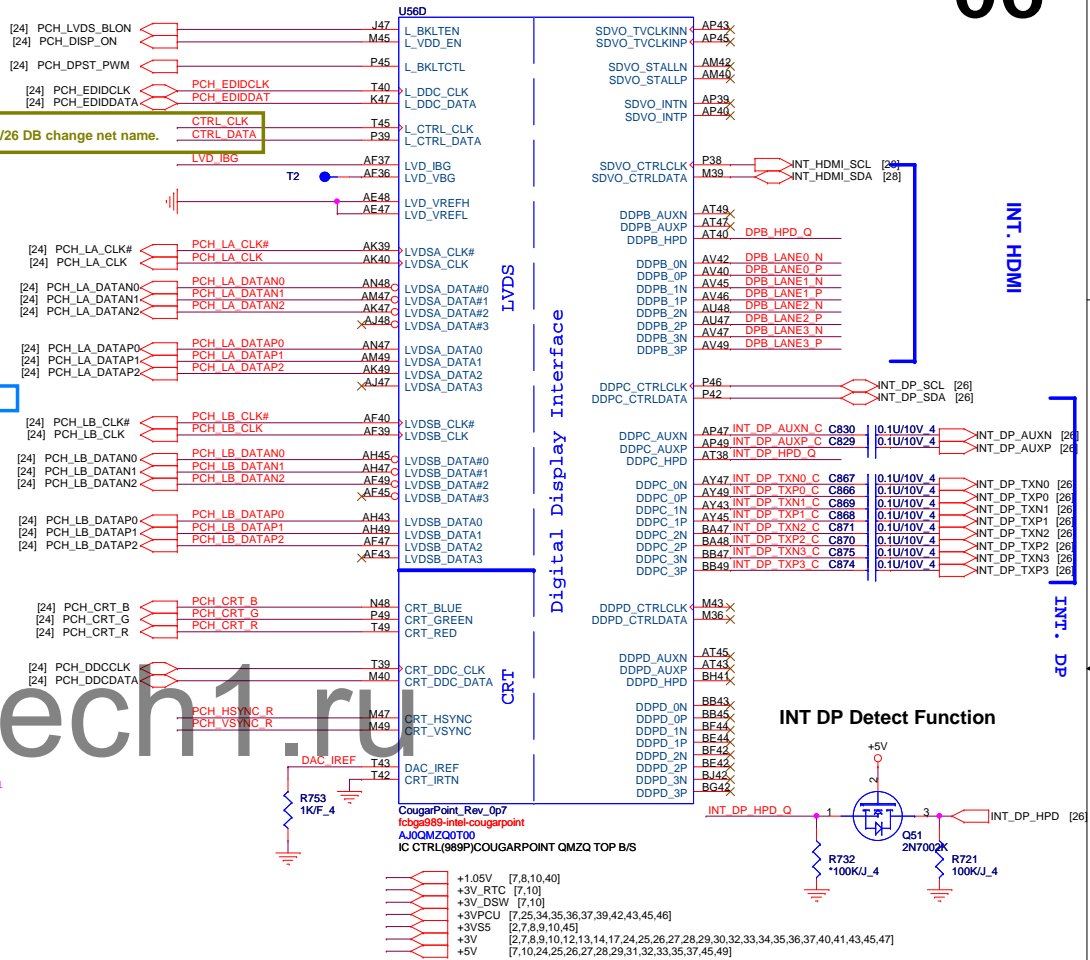
CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 4/4 (GND)	1A
Date: Tuesday, August 10, 2010	Sheet 5 of 49	





NB5/RD2

Size	Document Number
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NB5/RD2

Date: Tuesday, August 10, 2010 Sheet 7 of 49

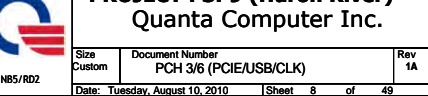
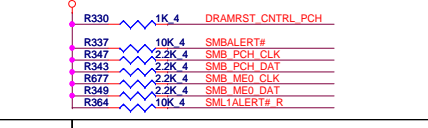
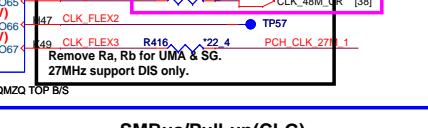
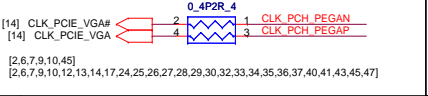
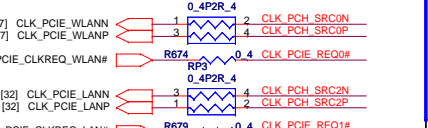
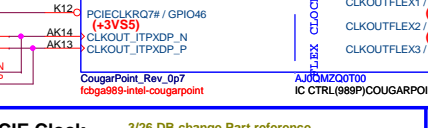
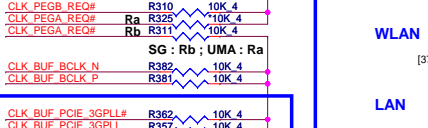
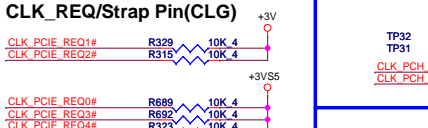
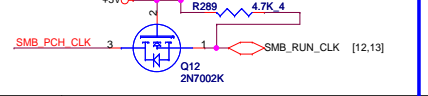
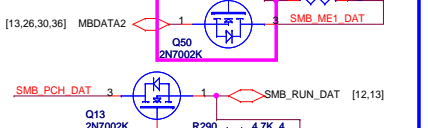
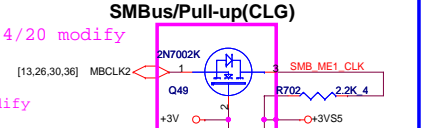
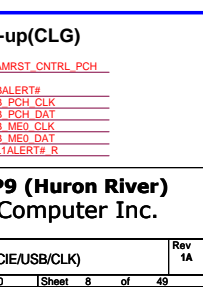
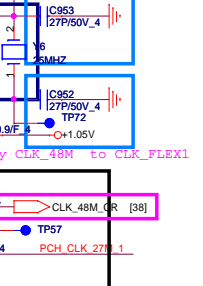
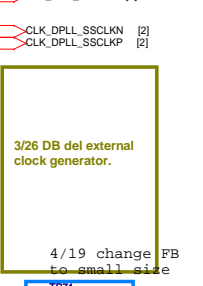
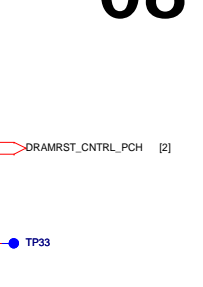
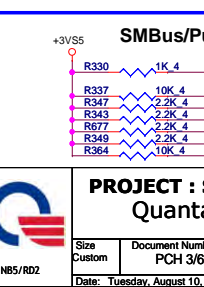
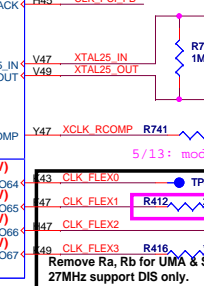
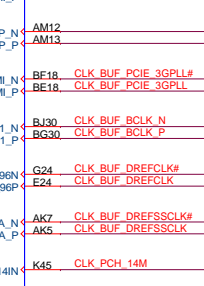
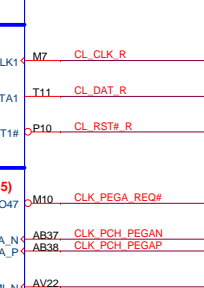
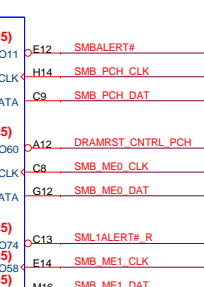
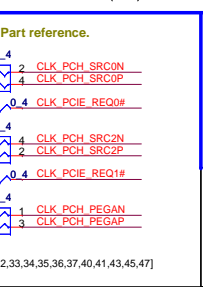
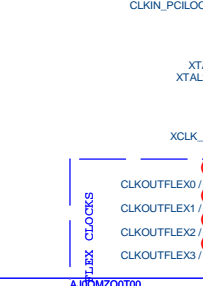
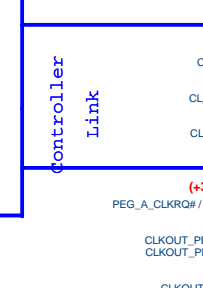
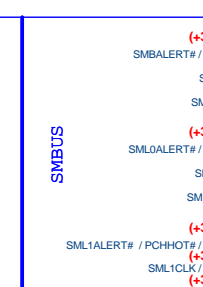
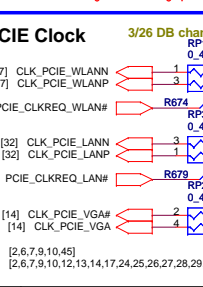
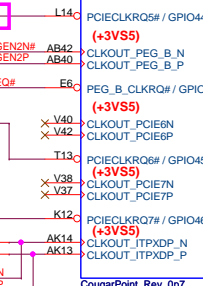
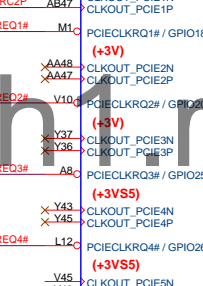
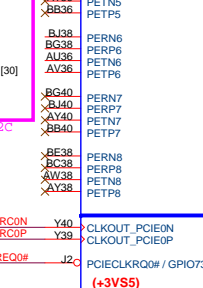
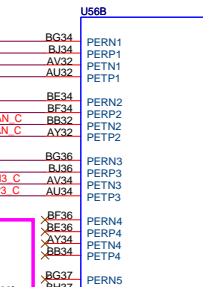
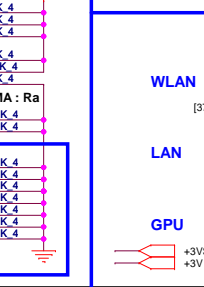
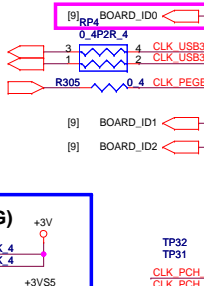
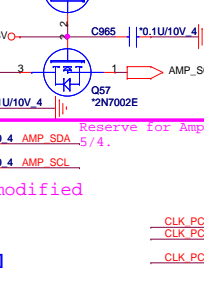
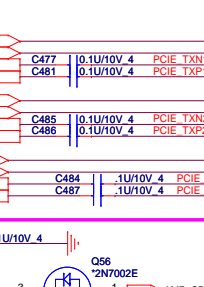
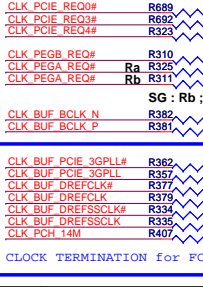
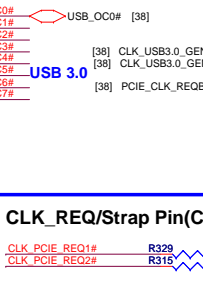
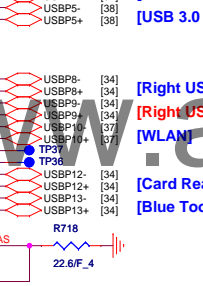
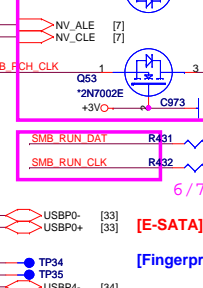
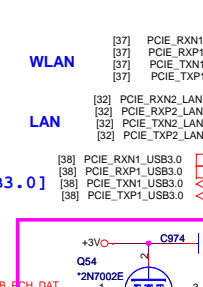
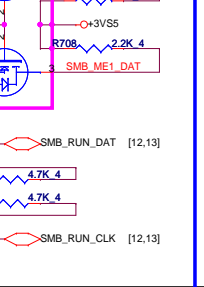
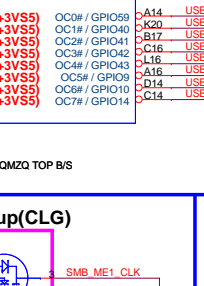
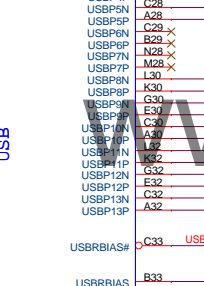
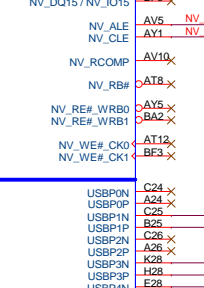
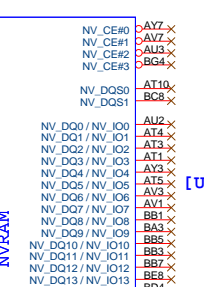
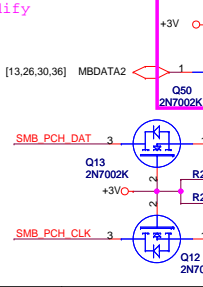
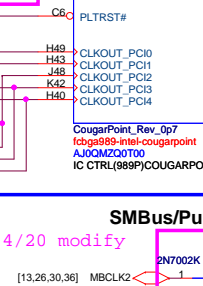
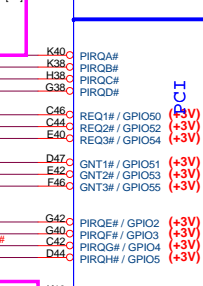
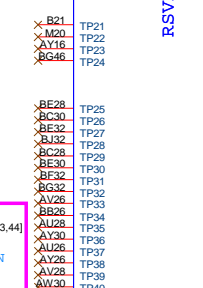
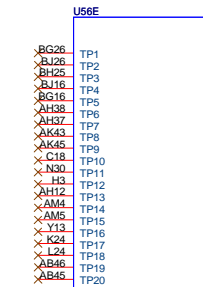
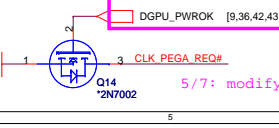
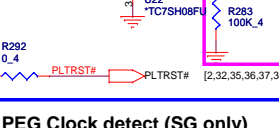
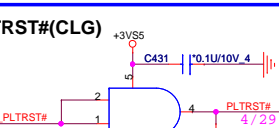
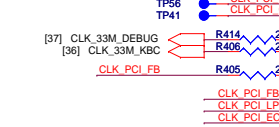
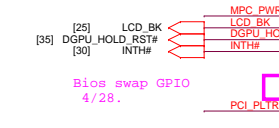
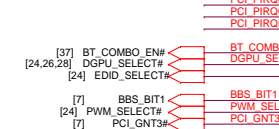
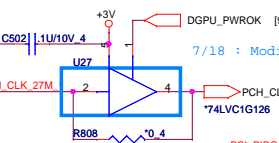
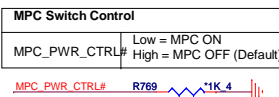
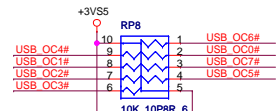
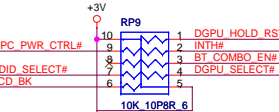
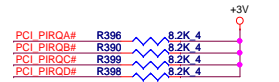
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit						
SPKR	Different from Calpella No reboot mode setting	PWROK	0 = Default (weak pull-up mode 20K) 1 = Setting to No-Reboot mode							
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)							
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up							
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)							
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>0</td><td>SPI LPC</td></tr></tbody></table>	GNT1#	GNT0#	Boot Location	1	0	SPI LPC	
GNT1#	GNT0#	Boot Location								
1	0	SPI LPC								
GPIO19	Different from Calpella Boot BIOS Selection 0 [bit-0]	PWROK								
GNT2# / GPIO53	ESi strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN						
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)							
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm 4/30 reserve.							
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V							
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)							
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)							
GPIO28	Different from Calpella On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)							
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable							

Cougar Point-M (PCI,USB,NVRAM)

Cougar Point-M (PCI-E,SMBUS,CLK)

PCI/USBOC# Pull-up(CLG)



CougarPoint_Rev_07
fcbg989-inl-cougarpoint
AJ0M200700
IC CTRL(989P) COUGARPOINT QM2Q TOP B/S

CougarPoint_Rev_07
fcbg989-inl-cougarpoint
AJ0M200700
IC CTRL(989P) COUGARPOINT QM2Q TOP B/S

4/20 modify

13,26,30,36

MDATA2

SMB_PCH_DAT

Q13 2N7002K

R290 4.7K 4

R289 4.7K 4

Q12 2N7002K

CLK_PCIE_REQ# R329 10K 4

CLK_PCIE_REQ# R315 10K 4

CLK_PCIE_REQ# R689 10K 4

CLK_PCIE_REQ# R692 10K 4

CLK_PCIE_REQ# R323 10K 4

CLK_PCIE_REQ# R310 10K 4

CLK_PCIE_REQ# R311 10K 4

CLK_PCIE_REQ# R312 10K 4

CLK_PCIE_REQ# R313 10K 4

CLK_PCIE_REQ# R329 10K 4

CLK_PCIE_REQ# R315 10K 4

CLK_PCIE_REQ# R689 10K 4

CLK_PCIE_REQ# R692 10K 4

CLK_PCIE_REQ# R323 10K 4

CLK_PCIE_REQ# R310 10K 4

CLK_PCIE_REQ# R311 10K 4

CLK_PCIE_REQ# R312 10K 4

CLK_PCIE_REQ# R313 10K 4

CLK_PCIE_REQ# R329 10K 4

CLK_PCIE_REQ# R315 10K 4

CLK_PCIE_REQ# R689 10K 4

CLK_PCIE_REQ# R692 10K 4

CLK_PCIE_REQ# R323 10K 4

CLK_PCIE_REQ# R310 10K 4

CLK_PCIE_REQ# R311 10K 4

CLK_PCIE_REQ# R312 10K 4

CLK_PCIE_REQ# R313 10K 4

5/7: modify

Q14 2N7002

R405 22.4

R406 22.4

SG: Rb: UMA: Ra

CLK_BUF_BOLK_N

CLK_BUF_BOLK_P

CLK_BUF_BOLK_N

CLK_PCIE_REQ# R329 10K 4

CLK_PCIE_REQ# R315 10K 4

CLK_PCIE_REQ# R689 10K 4

CLK_PCIE_REQ# R692 10K 4

CLK_PCIE_REQ# R329 10K 4

CLK_PCIE_REQ# R315 10K 4

CLK_PCIE_REQ# R689 10K 4

CLK_PCIE_REQ# R692 10K 4

4/29 modify

13,26,30,36

MDATA2

SMB_PCH_DAT

Q13 2N7002K

R290 4.7K 4

R289 4.7K 4

Q12 2N7002K

Q14 2N7002

CLK_PCIE_REQ# R329 10K 4

CLK_PCIE_REQ# R315 10K 4

CLK_PCIE_REQ# R689 10K 4

CLK_PCIE_REQ# R692 10K 4

CLK_PCIE_REQ# R323 10K 4

CLK_PCIE_REQ# R310 10K 4

CLK_PCIE_REQ# R311 10K 4

CLK_PCIE_REQ# R312 10K 4

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CLK_PCIE_REQ# R315 10K 4

CLK_PCIE_REQ# R689 10K 4

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CLK_PCIE_REQ# R689 10K 4

CLK_PCIE_REQ# R692 10K 4

CLK_PCIE_REQ# R323 10K 4

CLK_PCIE_REQ# R310 10K 4

CLK_PCIE_REQ# R311 10K 4

CLK_PCIE_REQ# R312 10K 4

CLK_PCIE_REQ# R313 10K 4

4/20 modify

13,26,30,36

MDATA2

SMB_PCH_DAT

Q13 2N7002K

R290 4.7K 4

R289 4.7K 4

Q12 2N7002K

Q14 2N7002

CLK_PCIE_REQ# R329 10K 4

CLK_PCIE_REQ# R315 10K 4

CLK_PCIE_REQ# R689 10K 4

CLK_PCIE_REQ# R692 10K 4

CLK_PCIE_REQ# R323 10K 4

CLK_PCIE_REQ# R310 10K 4

CLK_PCIE_REQ# R311 10K 4

CLK_PCIE_REQ# R312 10K 4

CLK_PCIE_REQ# R313 10K 4

CLK_PCIE_REQ# R329 10K 4

CLK_PCIE_REQ# R315 10K 4

CLK_PCIE_REQ# R689 10K 4

CLK_PCIE_REQ# R692 10K 4

CLK_PCIE_REQ# R323 10K 4

CLK_PCIE_REQ# R310 10K 4

CLK_PCIE_REQ# R311 10K 4

CLK_PCIE_REQ# R312 10K 4

CLK_PCIE_REQ# R313 10K 4

CLK_PCIE_REQ# R329 10K 4

CLK_PCIE_REQ# R315 10K 4

CLK_PCIE_REQ# R689 10K 4

CLK_PCIE_REQ# R692 10K 4

CLK_PCIE_REQ# R323 10K 4

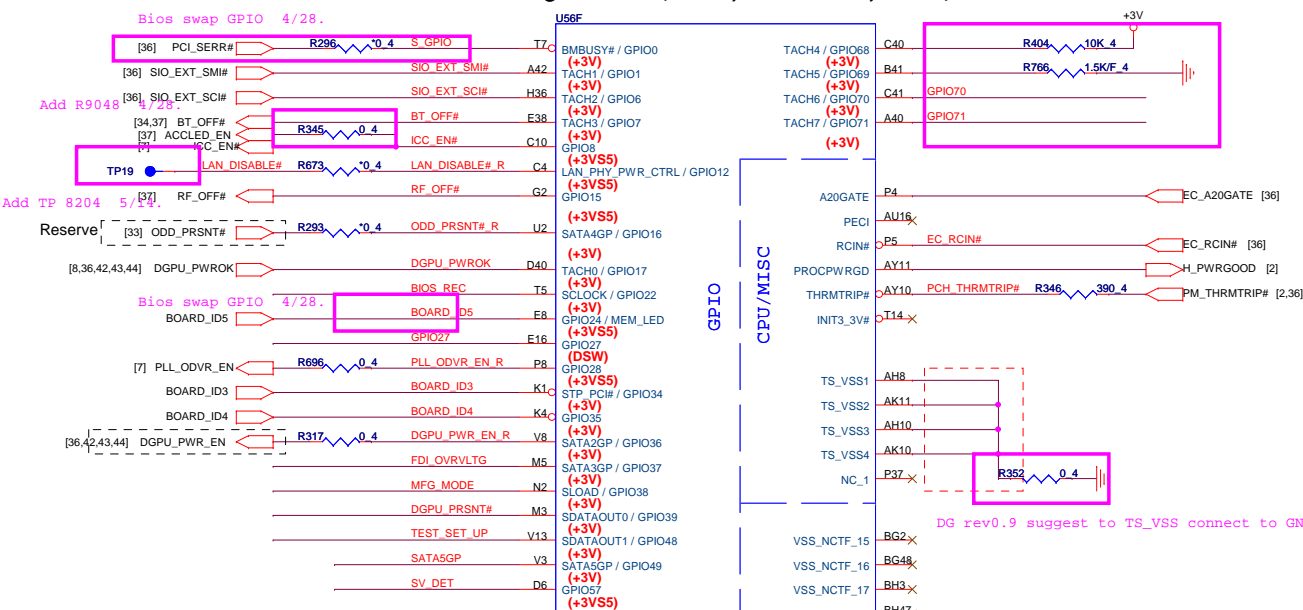
CLK_PCIE_REQ# R310 10K 4

CLK_PCIE_REQ# R311 10K 4

CLK_PCIE_REQ# R312 10K 4

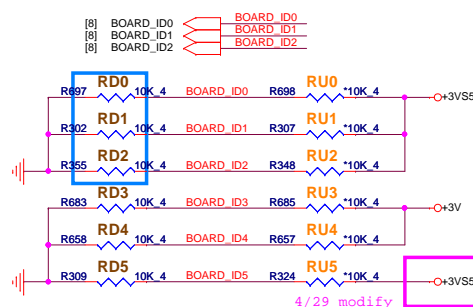
CLK_PCIE_REQ# R313 10K 4

Cougar Point (GPIO,VSS_NCTF,RSVD)



DG rev0.9 suggest to TS_VSS connect to GND 4/23

Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
SP9 2D	0	0	0	0	0	0
SP9 3D	0	0	0	0	0	1



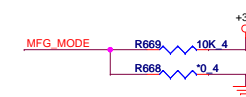
8/2 SI Modify

4/29 modify

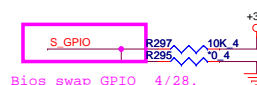
Clock Gen Power OK (CLG)

3/26 DB del external clock generator.

MFG-TEST

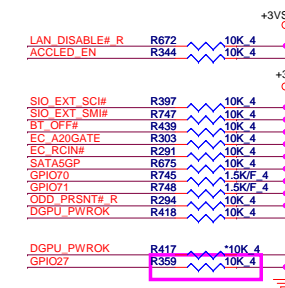


SGPIO

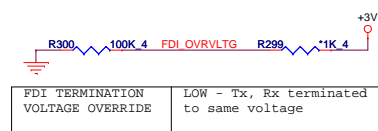
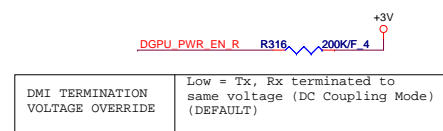
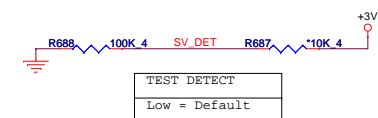
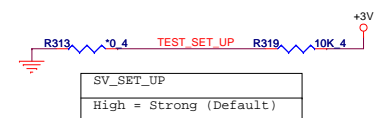
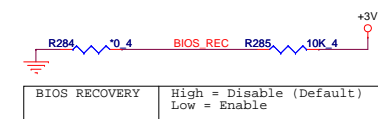
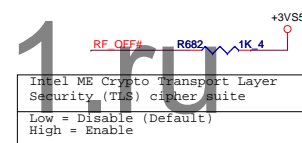


Bios swap GPIO 4/28.

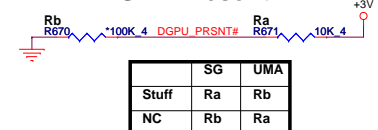
GPIO Pull-up/Pull-down(CLG)



5/4 modify



GFX Present



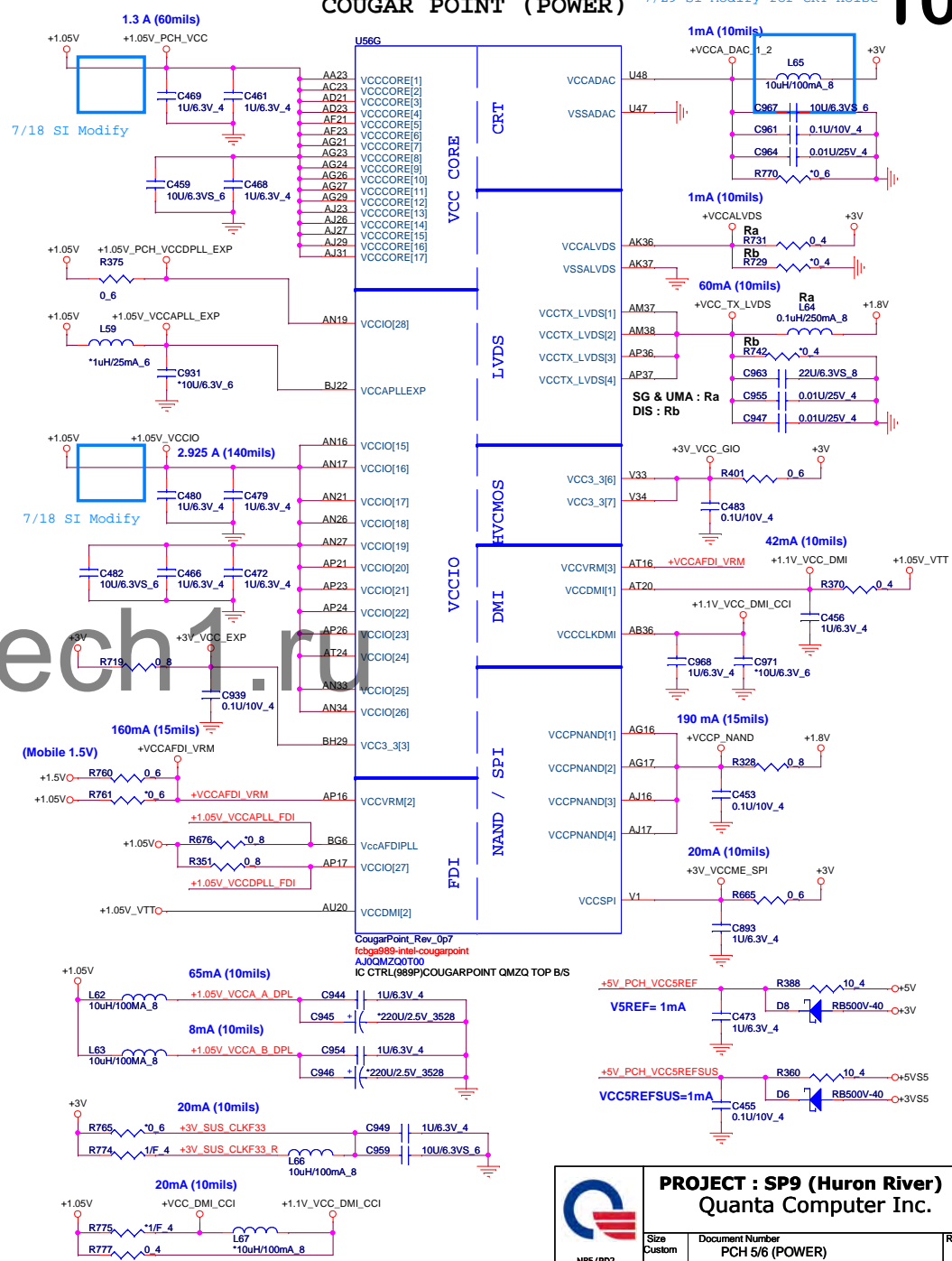
	SG	UM
Stuff	Ra	Rb
NC	Rb	Ra



PROJECT : SP9 (Huron River)
Quanta Computer Inc.

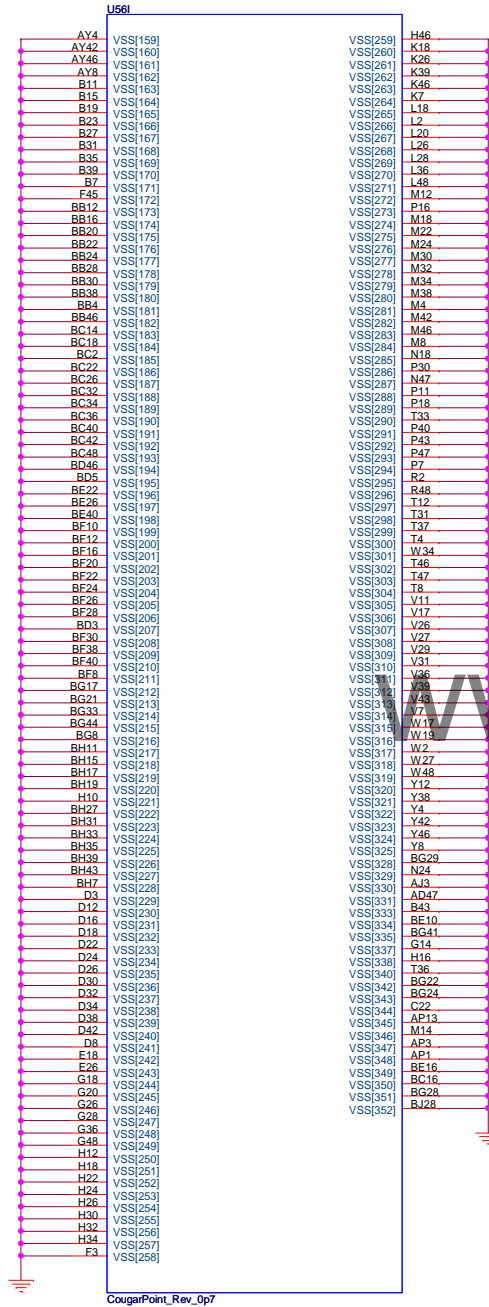
Size Custom	Document Number PCH 4/6 (GPIO/MISC)	Rev 1A
Date: Tuesday, August 10, 2010		Sheet 9 of 49

COUGAR POINT (POWER)

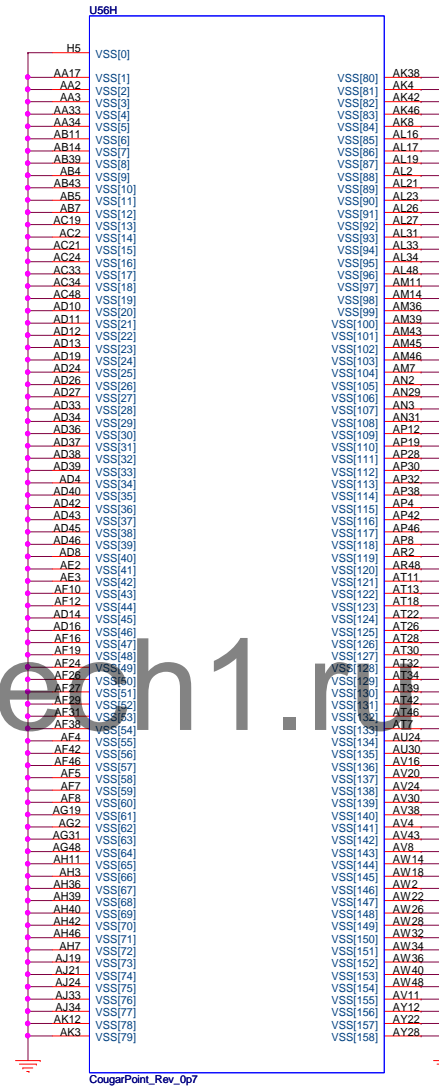


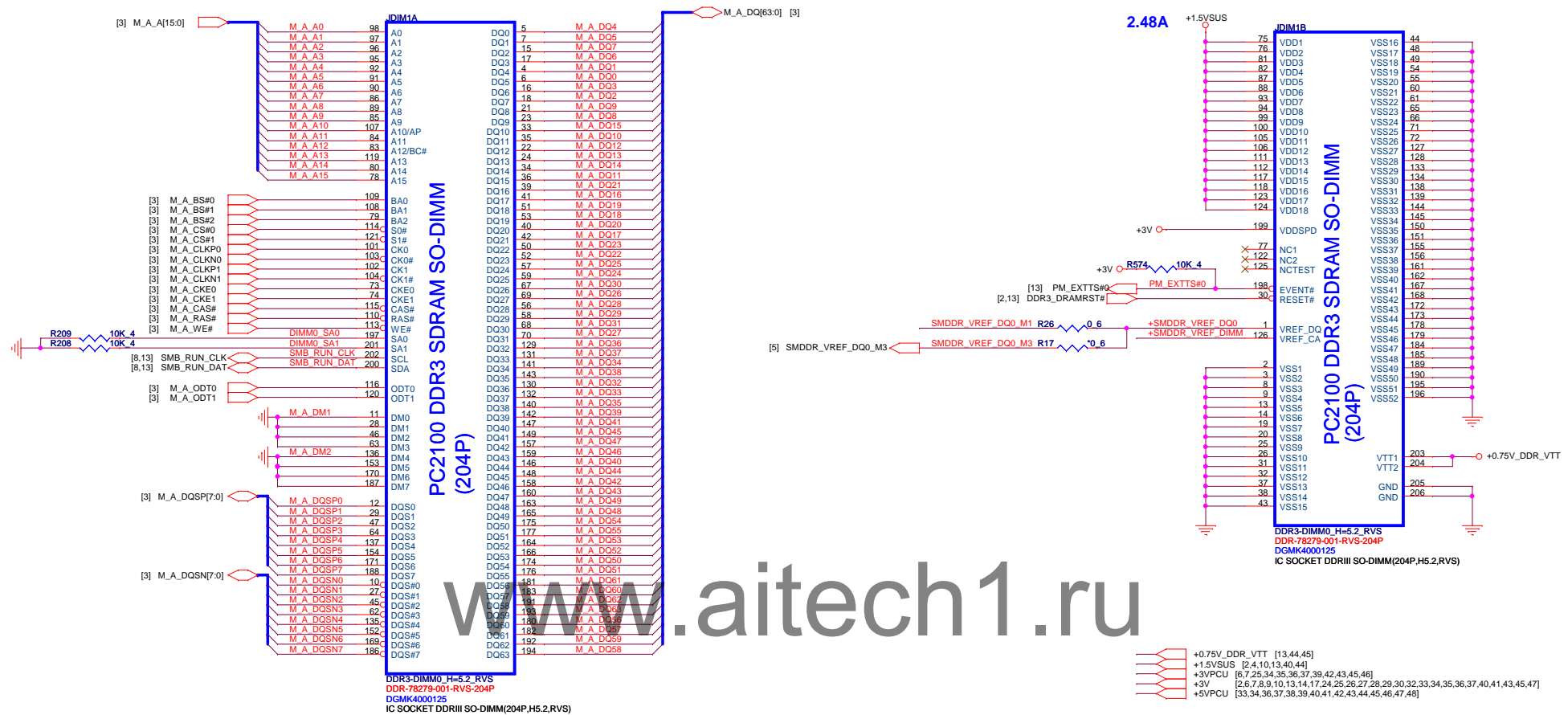
Size Custom	Document Number PCH 5/6 (POWER)	Rev 1A
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IBEX PEAK-M (GND)

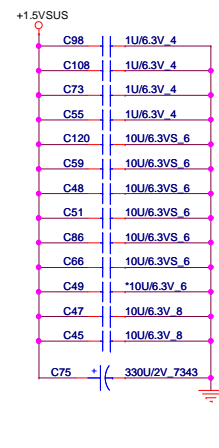


IBEX PEAK-M (GND)



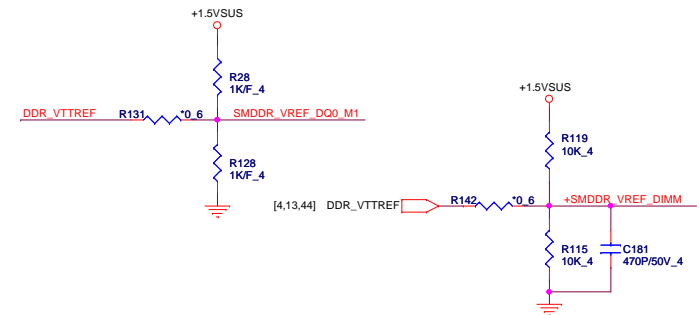


VREF DQ0 M2 Solution

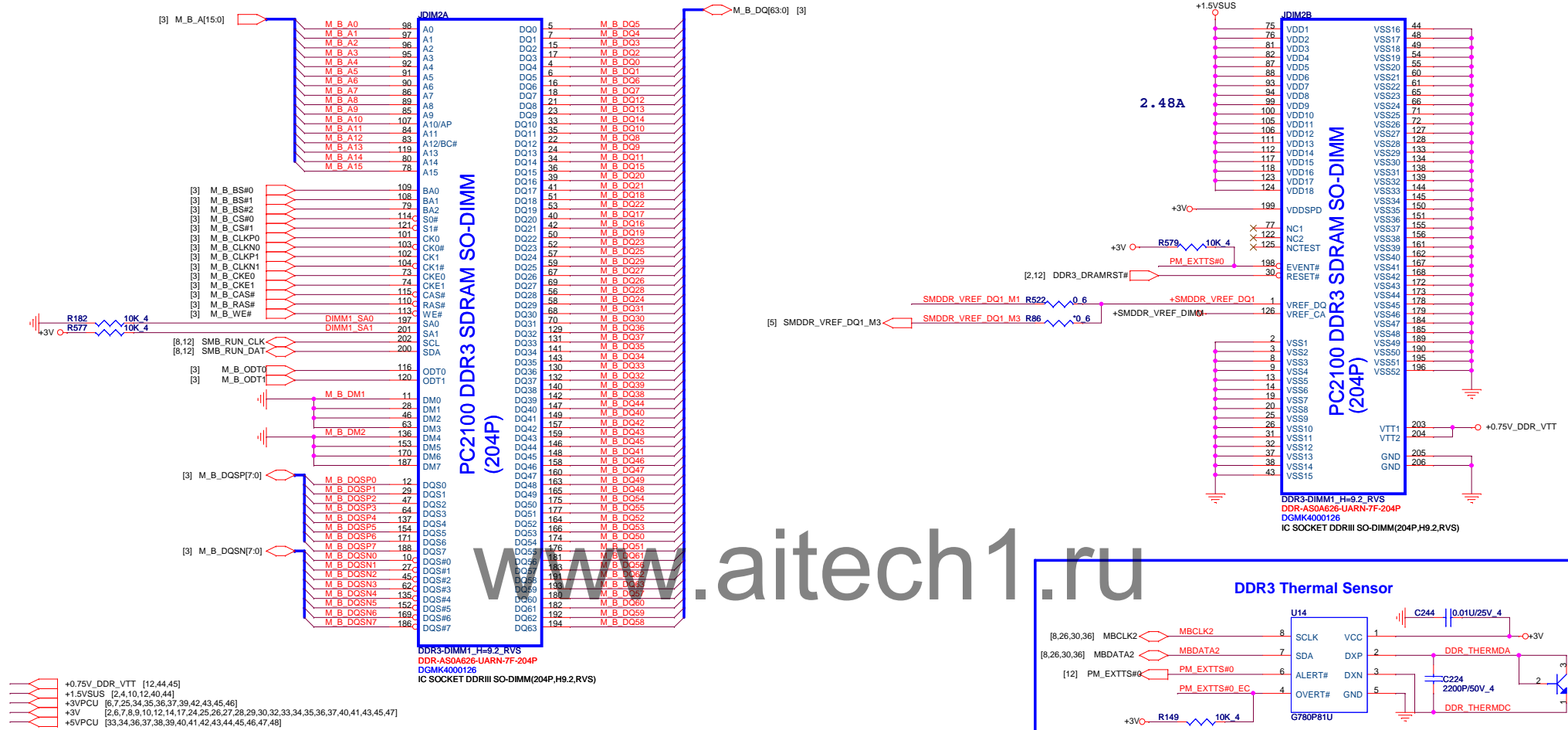


Place these Caps near So-Dimm0.

VREF DQ0 M1 Solution

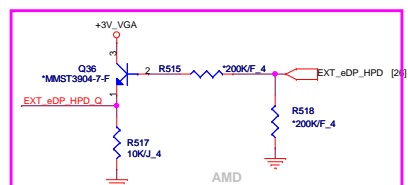


7/18 : Del M2 solution



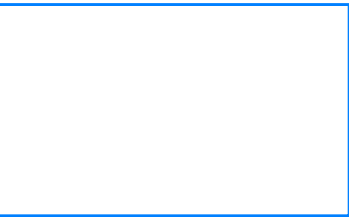






5/6 DB add.

7/19 SI Modify remove R541/R51/C664/C50



5/6 add for AMD
For LVDS

reserver for
internal thermal

PV change for EC request

5/20 add for AMD

PV Add CTF function.

3D support

3D support

3D support

3D support

3D support

3D support

3D support

3D support

3D support

3D support

3D support

3D support

3D support

3D support

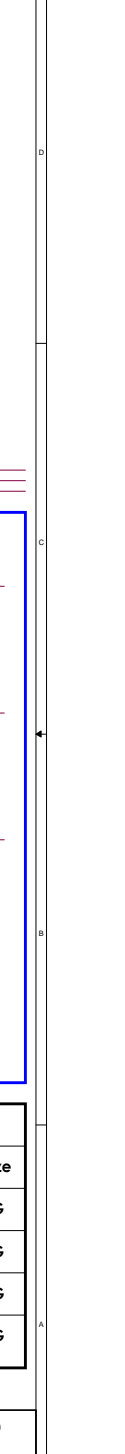
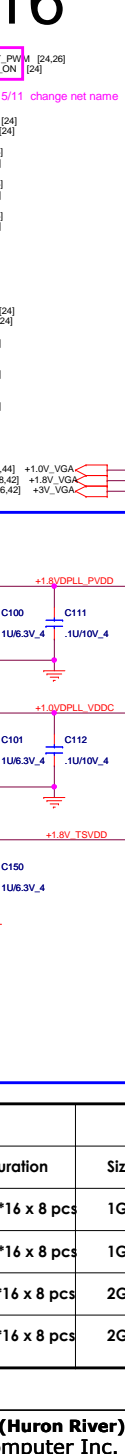
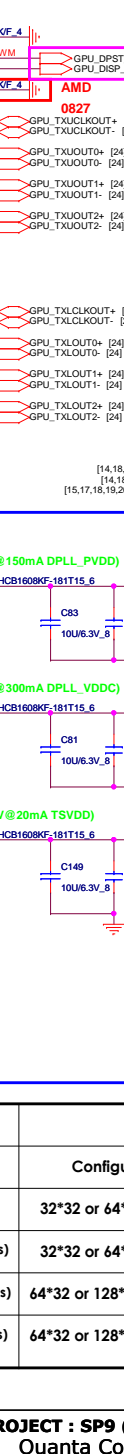
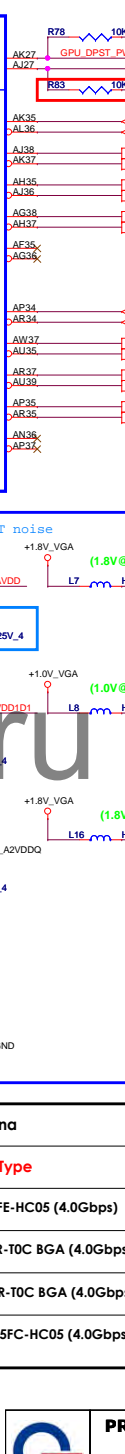
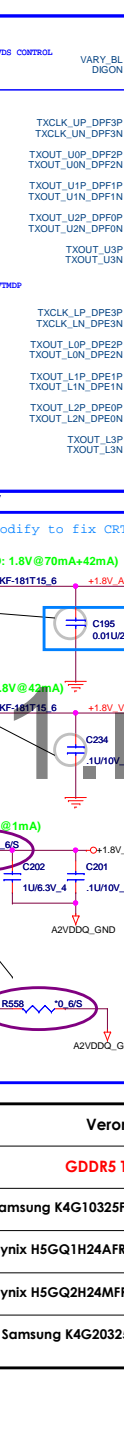
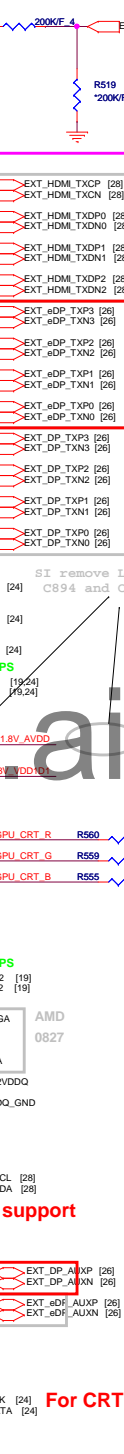
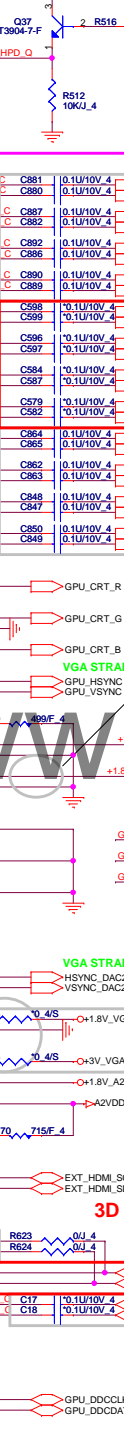
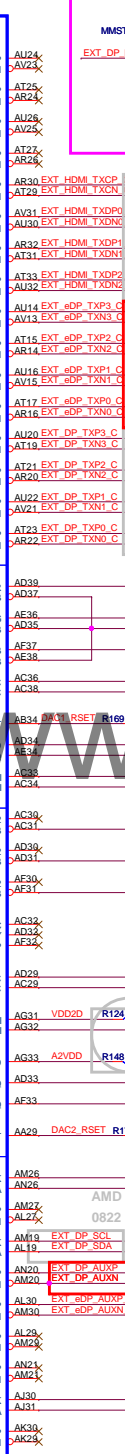
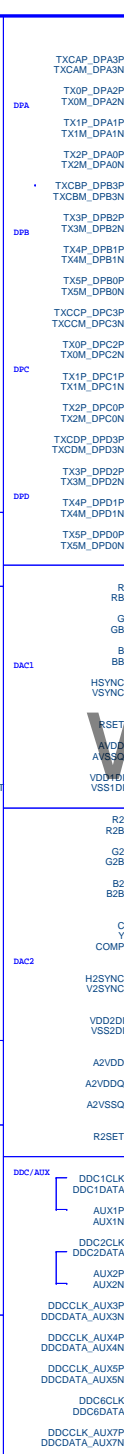
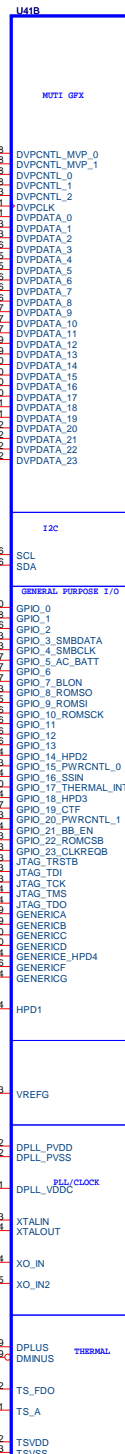
3D support

3D support

3D support

3D support

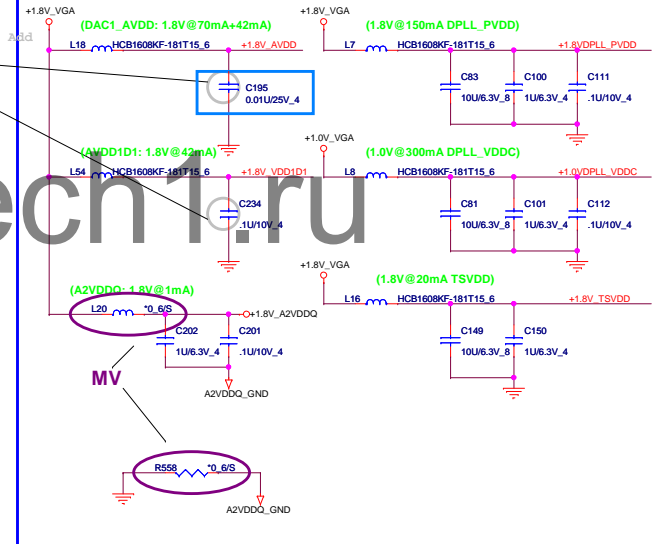
3D support



3D support
eDisplay port

Mini-display port

7/19 SI Modify to fix CRT noise



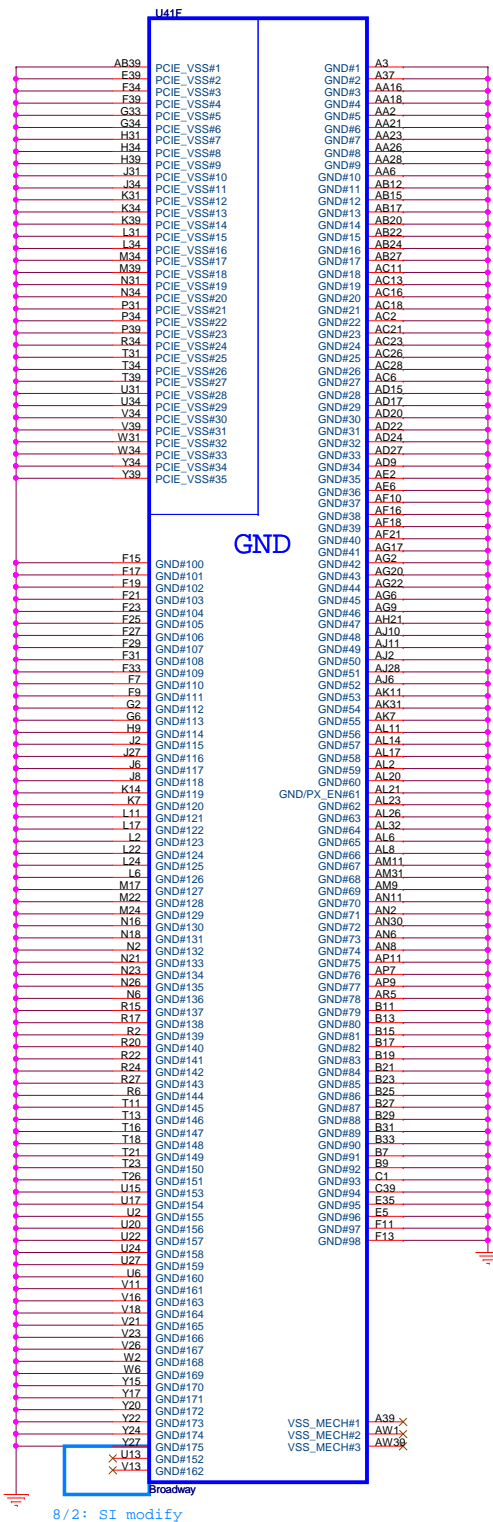
MEM ID	3	2	1	0	Verona		
DVPDATA	3	2	1	0	DDR5 Type	Configuration	Size
1	0	0	0	1	Samsung K4G10325FE-HC05 (4.0Gbps)	32*32 or 64*16 x 8 pcs	1G
2	0	0	1	0	Hynix H5GQ1H24AFR-TOC BGA (4.0Gbps)	32*32 or 64*16 x 8 pcs	1G
3	0	0	1	1	Hynix H5GQ2H24MFR-TOC BGA (4.0Gbps)	64*32 or 128*16 x 8 pcs	2G
4	0	1	0	0	Samsung K4G20325FC-HC05 (4.0Gbps)	64*32 or 128*16 x 8 pcs	2G



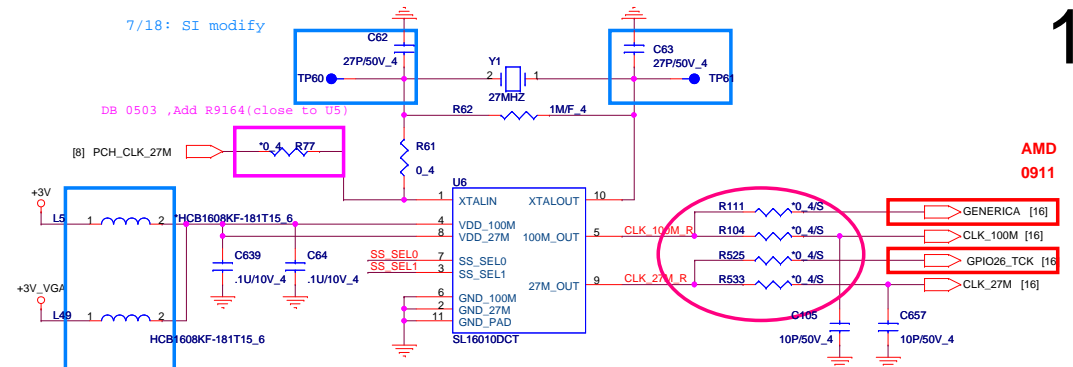
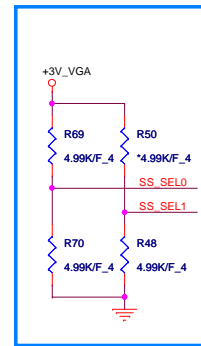
PROJECT : SP9 (Huron River)
Quanta Computer Inc.

Size Custom Document Number
ATI M97-M2 (DISPLAY) 3/5
Date: Tuesday, August 10, 2010 1 Sheet 16 of 49

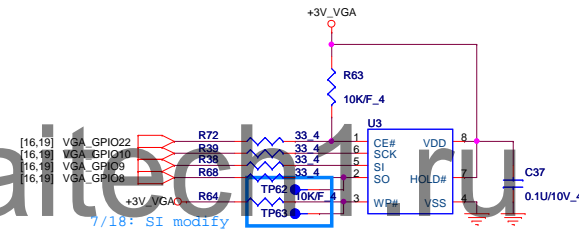
Rev 1A



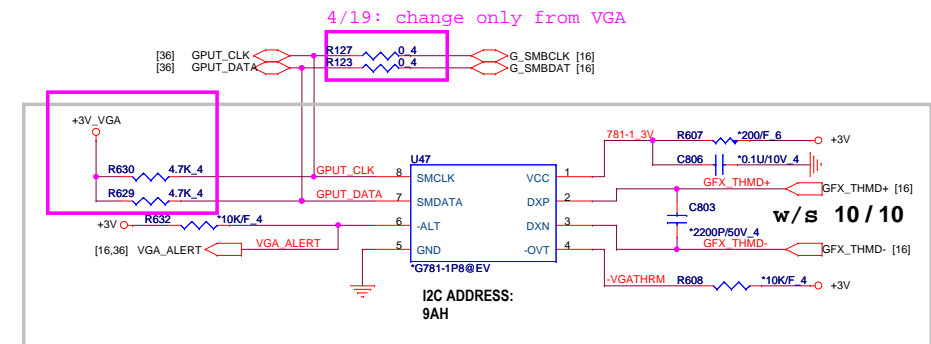
27MHz + 100Mhz OSC Option



Ext EEPROM



Thermal Sensor



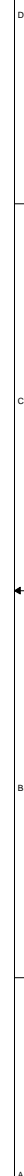
[2,6,7,8,9,10,12,13,14,24,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47]

[15,16,18,19,26,42]

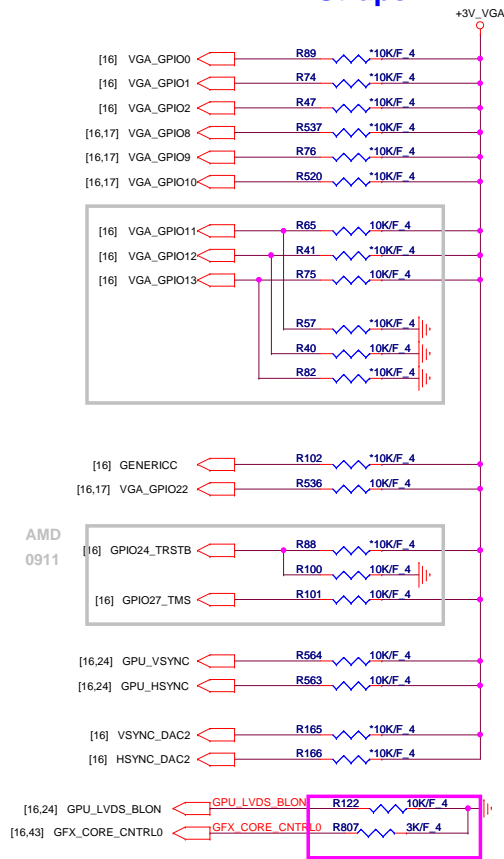


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Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATI M97(GND&Str&Ther)4/5	1A
Date: Tuesday, August 10, 2010	Sheet 17 of 49	



Straps



5/21 add pu down by AMD request.

Table 3-34 ROM Configurations

Manufacturer	Part Number	Size	CONFIG[2:0]
Atmel	AT25F512	512 kbit	001
	AT25F512A	512 kbit	010
	AT25F1024	1 Mbit	011
	AT25F1024A	1 Mbit	011
	AT25F2048	2 Mbit	011
	AT25F4096	4 Mbit	011
ST Microelectronics	M25P05A	512 kbit	100
	M25P10A	1 Mbit	101
	M25P20	2 Mbit	101
	M25P40	4 Mbit	101
	M25P80	8 Mbit	101
Silicon Storage Technology	SST25VF512	512 kbit	010
	SST25VF010	1 Mbit	011
	SST25VF020	2 Mbit	011
	SST25VF040	4 Mbit	011
Winbond Electronics Corporation	W45B512	512 kbit	110
	W45B012	1 Mbit	111
YMC	Y25LF05	512 kbit	010
	SA25C020	2 Mbit	011
PMC	Pm25LV512	512 kbit	100
	Pm25LV010	1 Mbit	101

Default

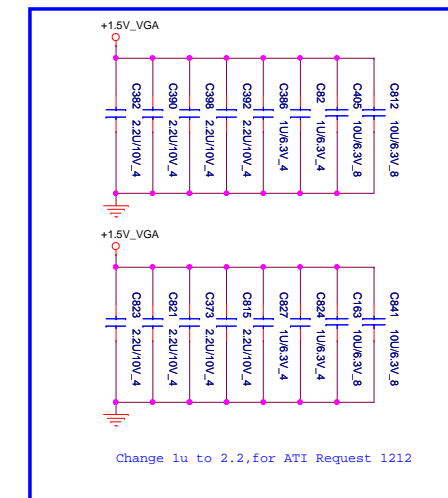
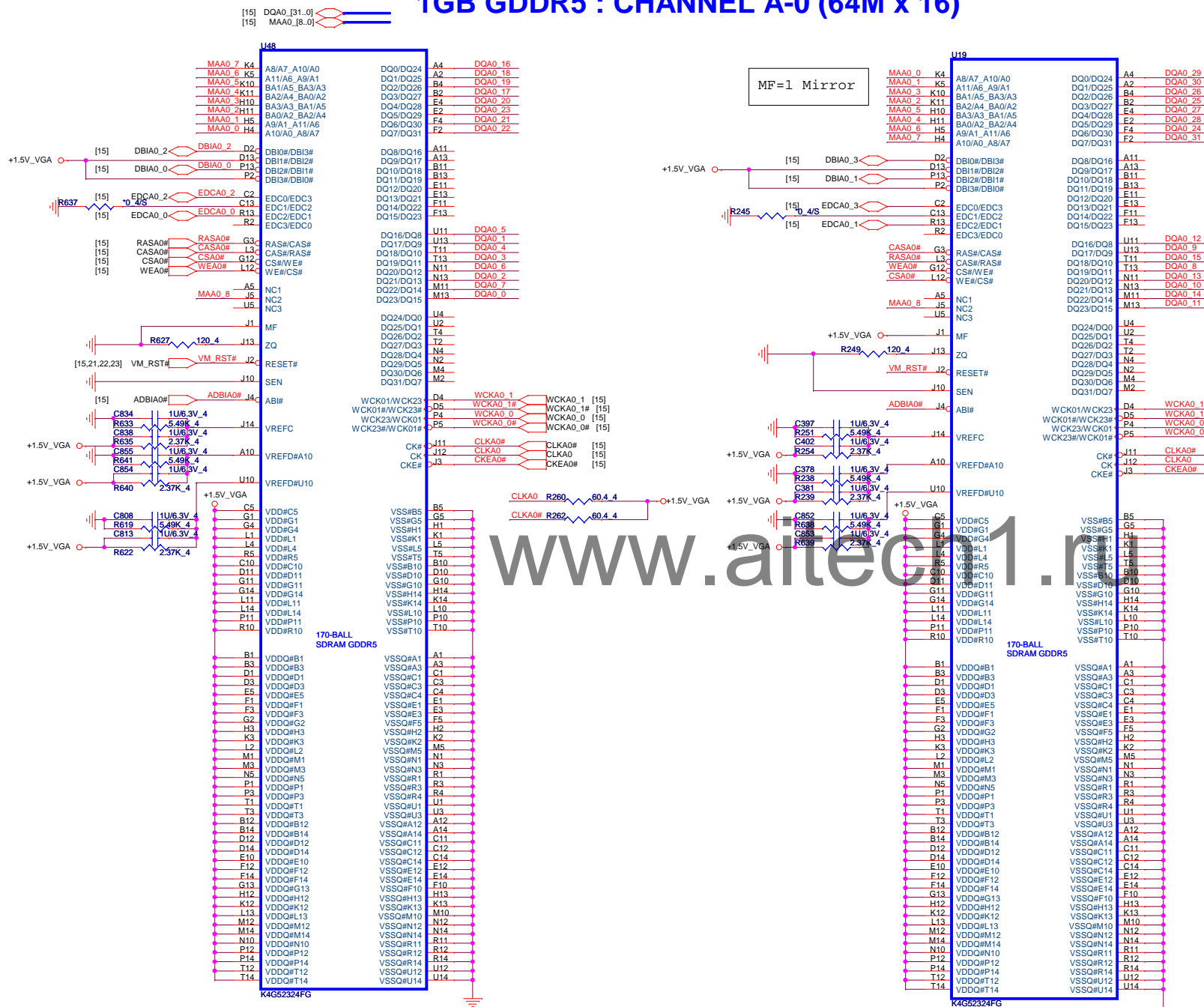
Strap Name	Pin	Straps Description	Default Value
TX_PWRS_ENB	GPIO0	GPIO[1:0]:Recommend to pulling up for PICE setting. GPIO_0:PCIE full TX output swing	
TX_DEEMPH_EN	GPIO1	GPIO_1:PCIE Transmitter DE-EMPHASIS enabled	
BIF_GEN2_EN	GPIO2	GPIO_2:System is using PCIE GEN1 can be let it NC(ASIC internal pull down) if Gen2 just pull up for PCIE 5GT/s support. (0=PCIE GNE1,2.5GT/s ; 1=PCIE GNE2,5GT/s)	
STRAP_BIF_CLK_PM_EN	GPIO8		
CONFIG[3] CONFIG[2] CONFIG[1] CONFIG[0]	GPIO9 GPIO13 GPIO12 GPIO11		
BIOS_ROM_EN	GPIO22	BIOS_ROM_EN(GPIO22)=1, then Config[2:0]=GPIO[13:12:11] defines the ROM type. (See table as below)	
AUDIO[0]	VSYN		
AUD(1) VSYNC_DAC2	HSYN V2SYN		
HSYN_DAC2	H2SYN		
	GENERICC		



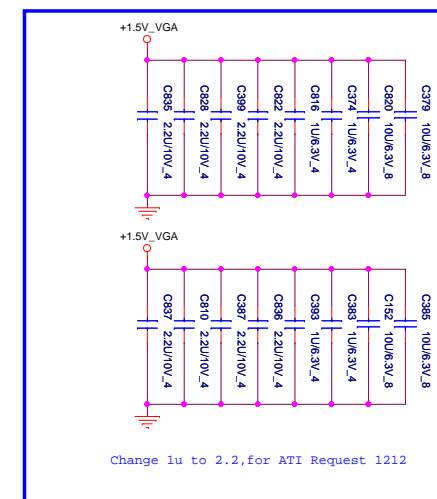
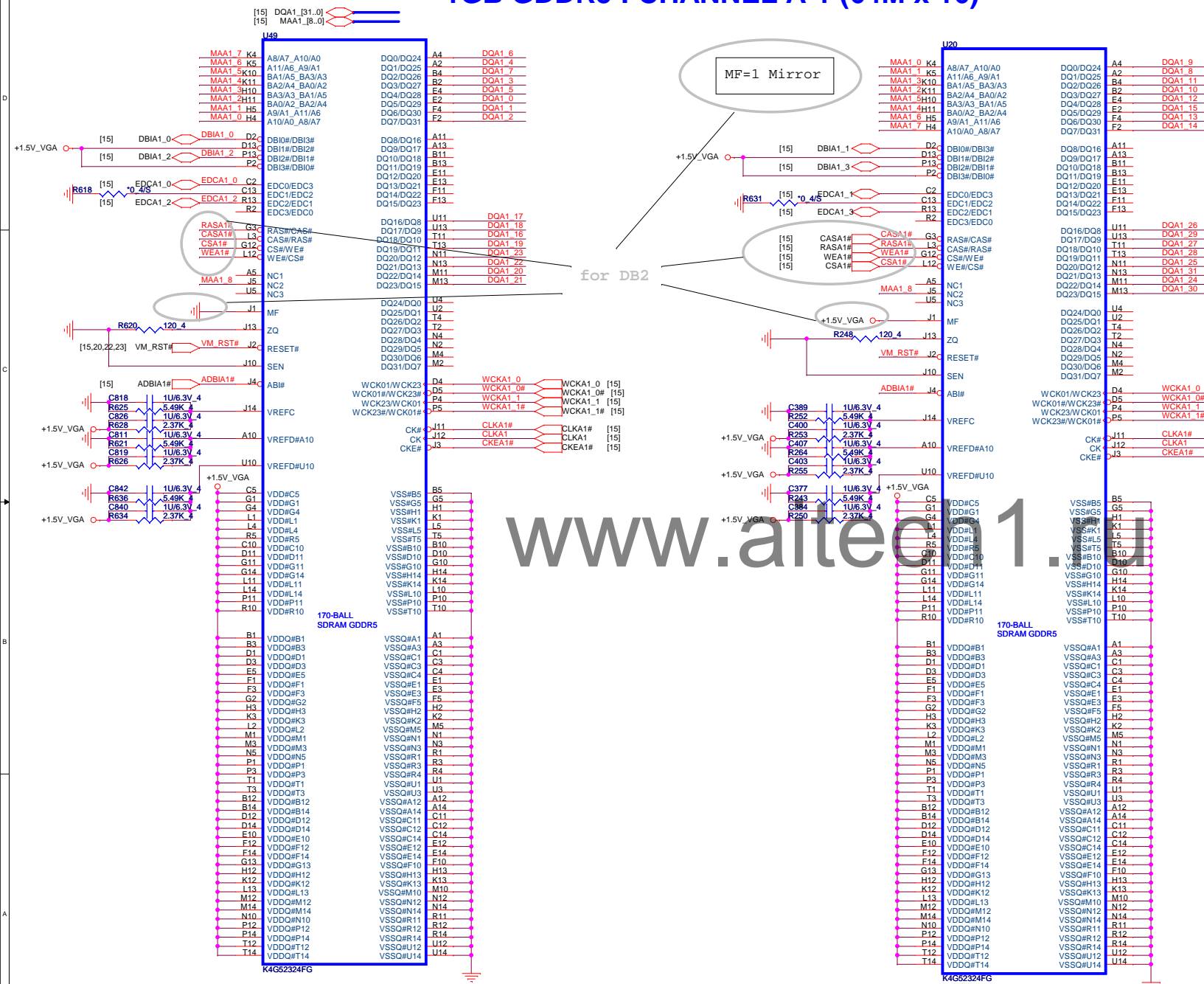
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Quanta Computer Inc.

Size Custom	Document Number VGA Core/+1.8VGF1.0VGF	Rev 1A
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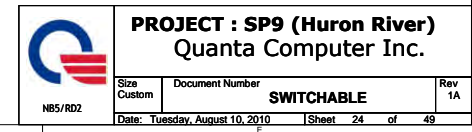
1GB GDDR5 : CHANNEL A-0 (64M x 16)

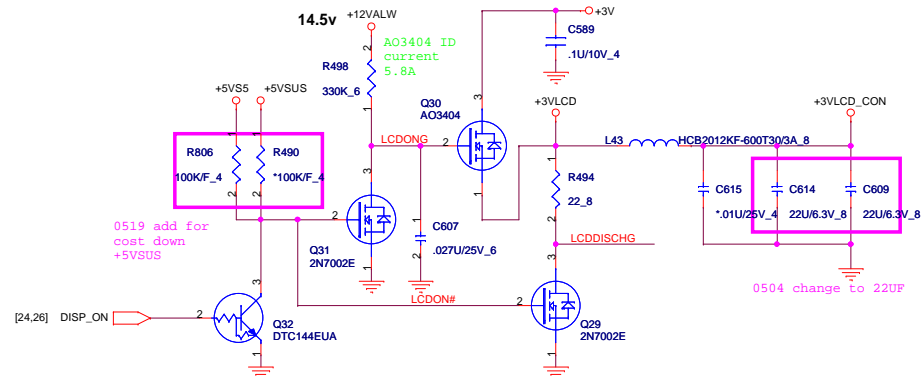
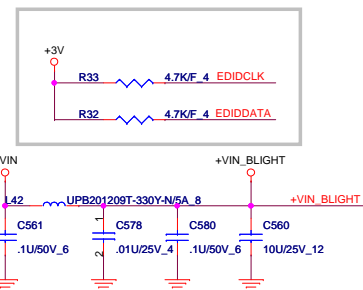


1GB GDDR5 : CHANNEL A-1 (64M x 16)

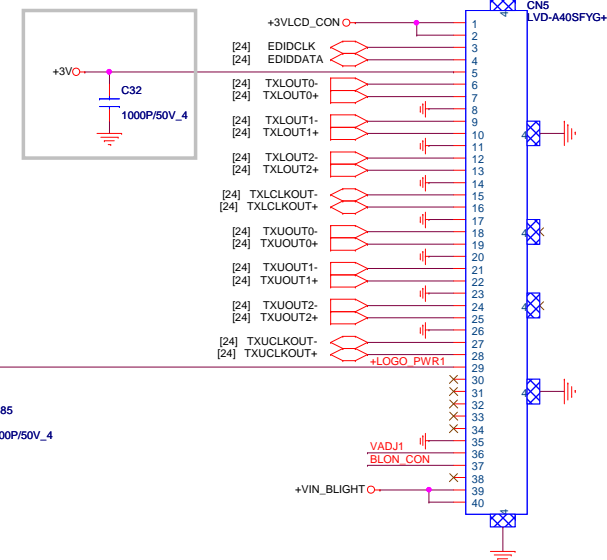


1GB GDDR5 : CHANNEL B-1 (64M x 16)

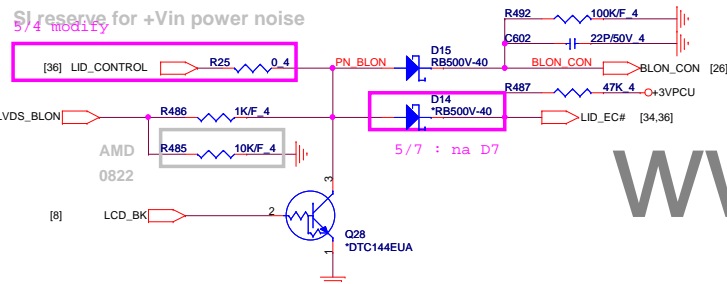


AMD
0822[2,6,7,8,9,10,12,13,14,17,24,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47]
[6,7,10,24,26,27,28,29,31,32,33,35,37,45,49]
[31,39,40,41,42,43,44,45,46,48]
[6,7,34,35,36,37,39,42,43,45,46]+3V
+5V
+VIN
+3VPCU

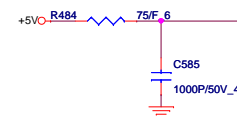
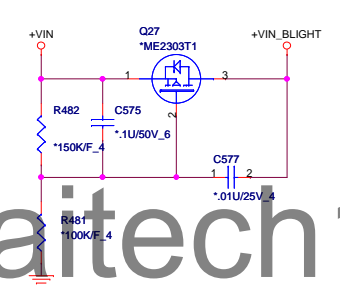
LCD



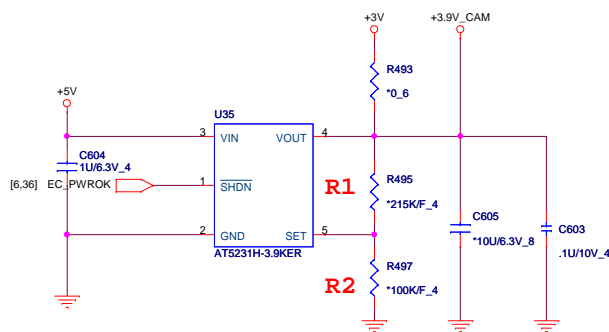
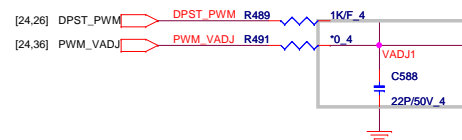
SI reserve for +Vin power noise



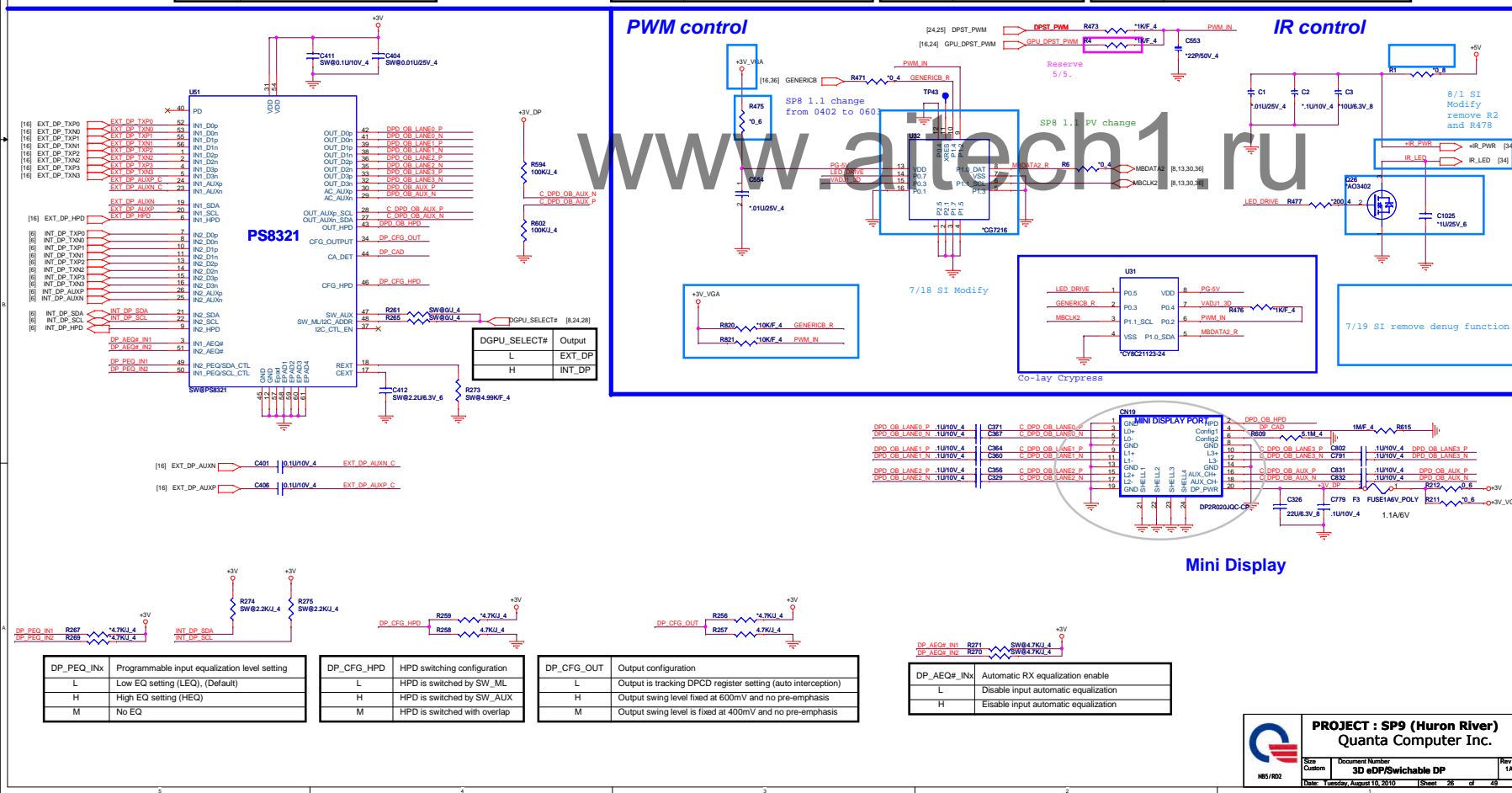
SI reserve for LCD soft start circuit

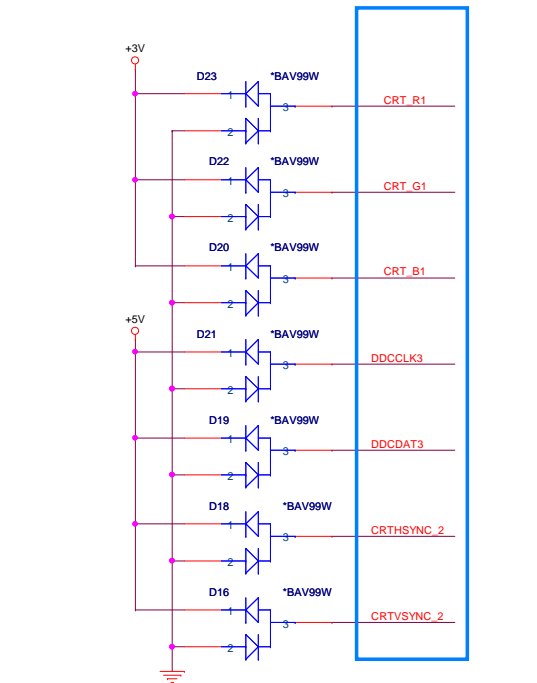
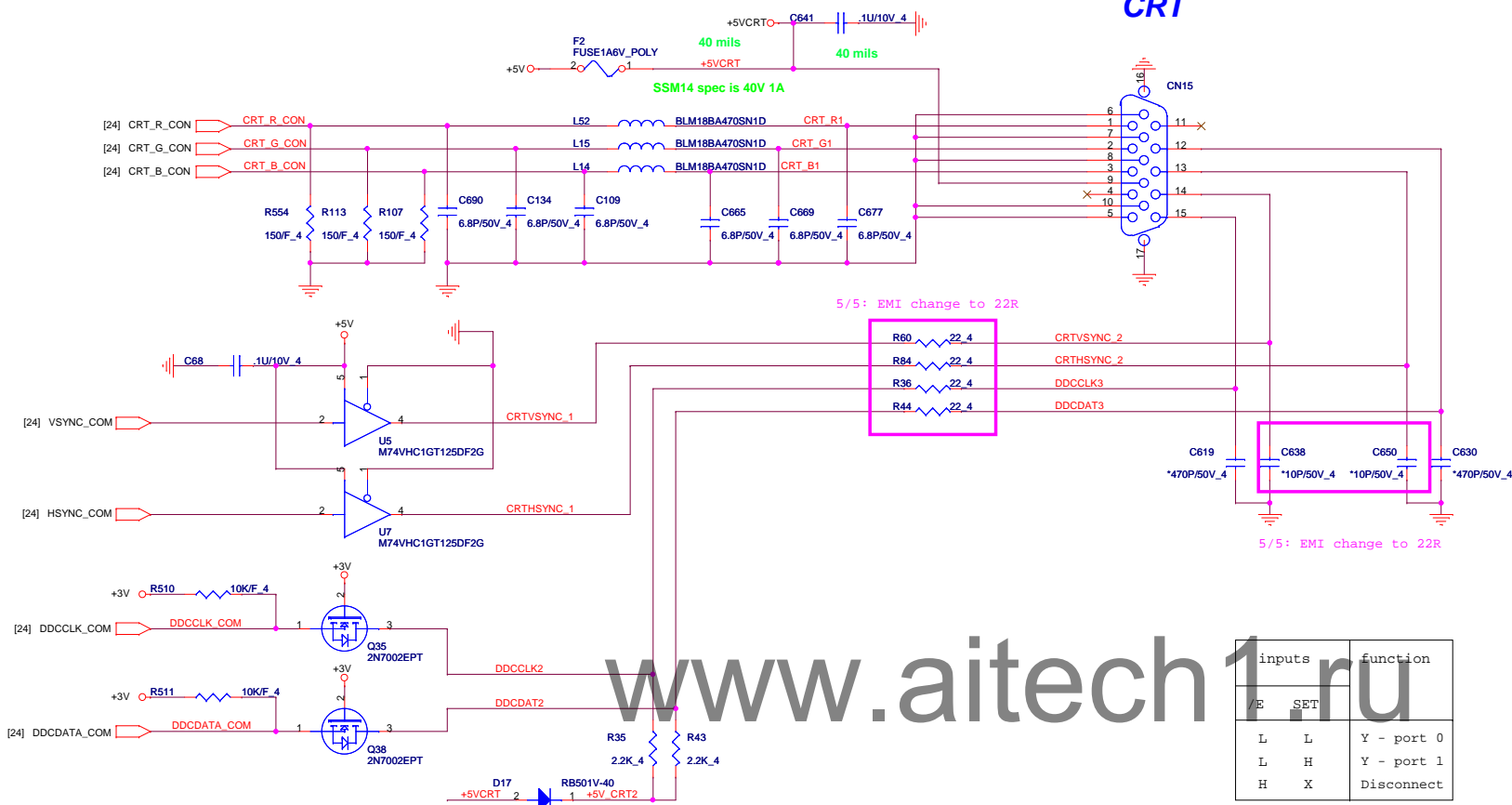


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$$V_{out} = 1.25(1 + R1/R2)$$



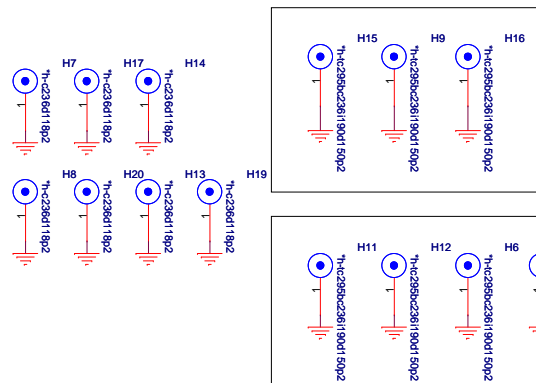


for GPU

SI ME change Footprint

SI for ME change footprint

SI add for PCH hole

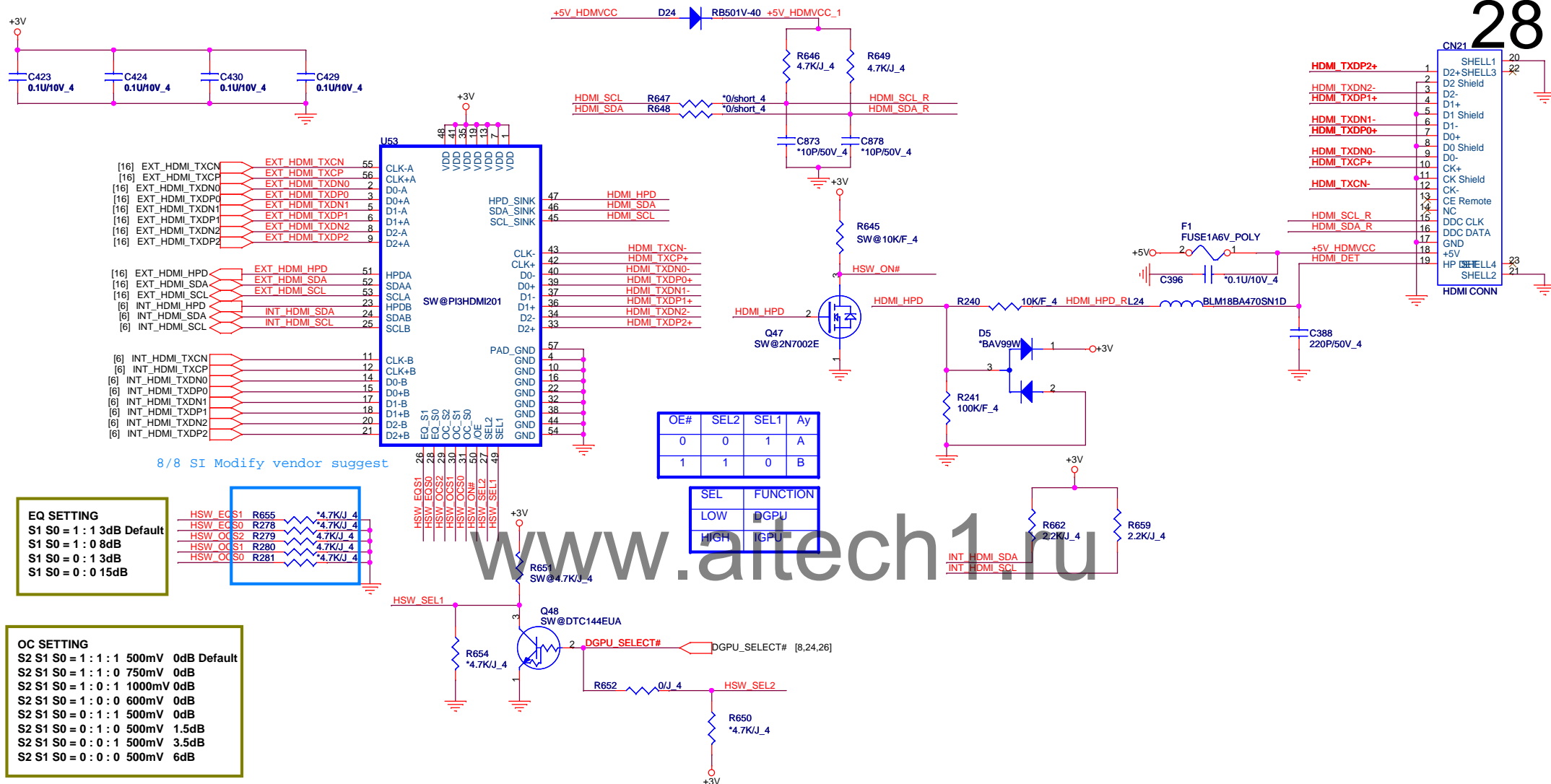


for CPU

Modify H5\H6,H11\H12\H13\H16\H17,H15 at 0506

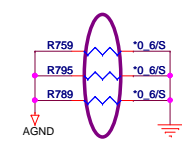
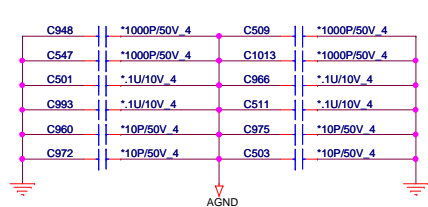
7/18 SI Modify

FOR LAYOUT



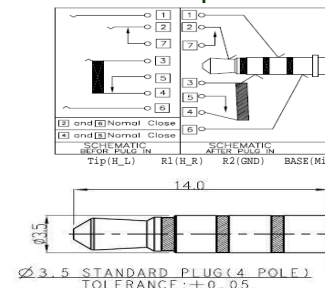
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7/18: SI Add



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SUBWOOFER

31

PV change R575 from 20K to 10K for HP request

SI add LDO for SUBWOOFER power

Change 4EQ to 2EQ

for PV

Sub-Woofer power

for DB2

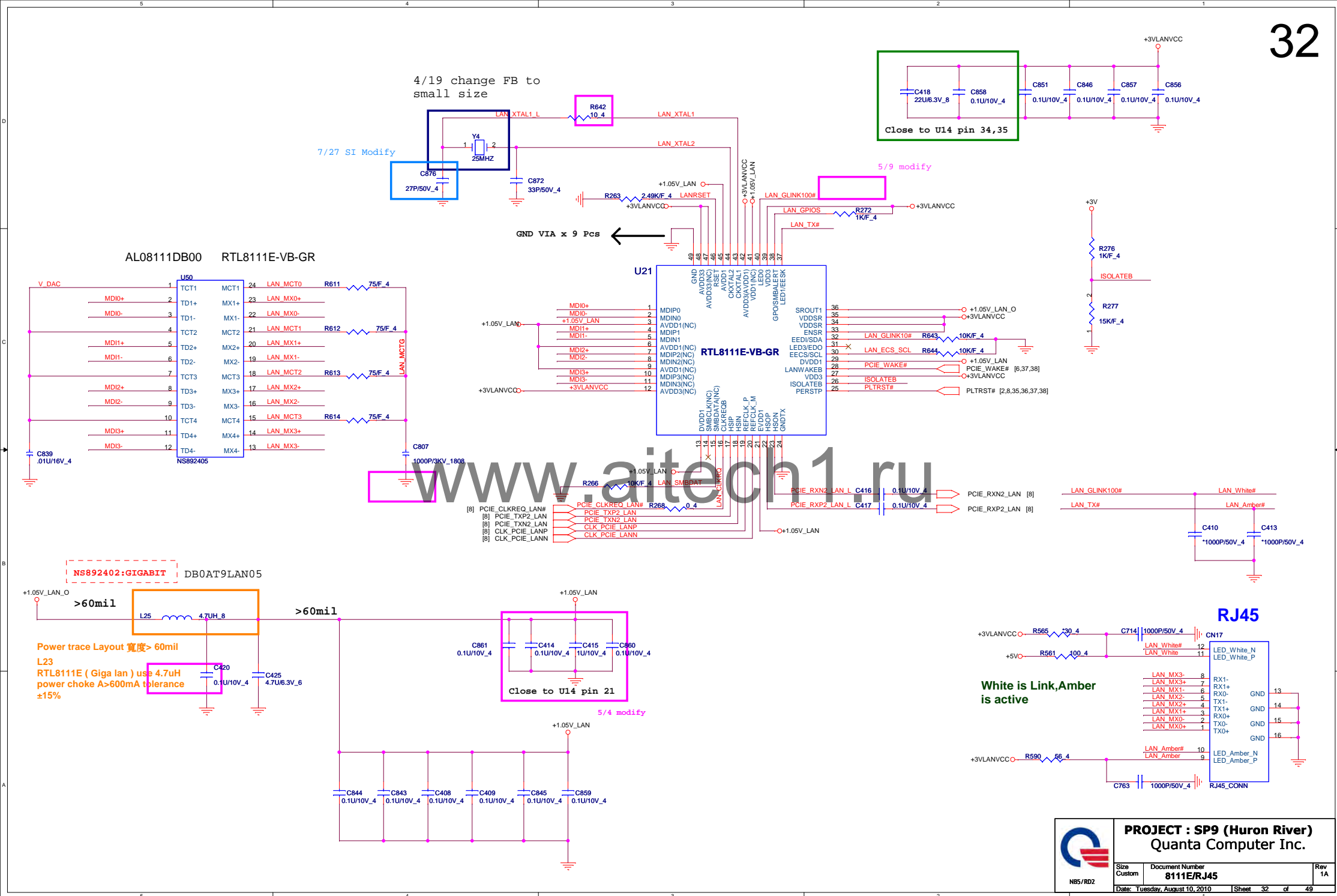
MV add R317

7/18 SI Modify
close to Connect

GAIN1	GAIN0	dB
0	0	20
0	1	26
1	0	32
1	1	36

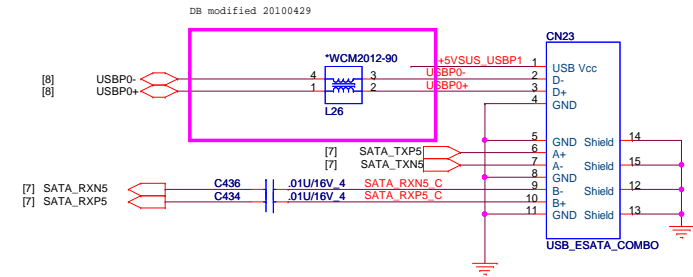
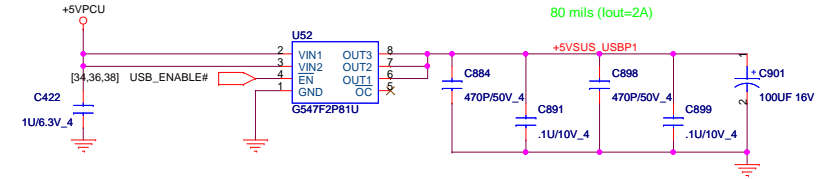
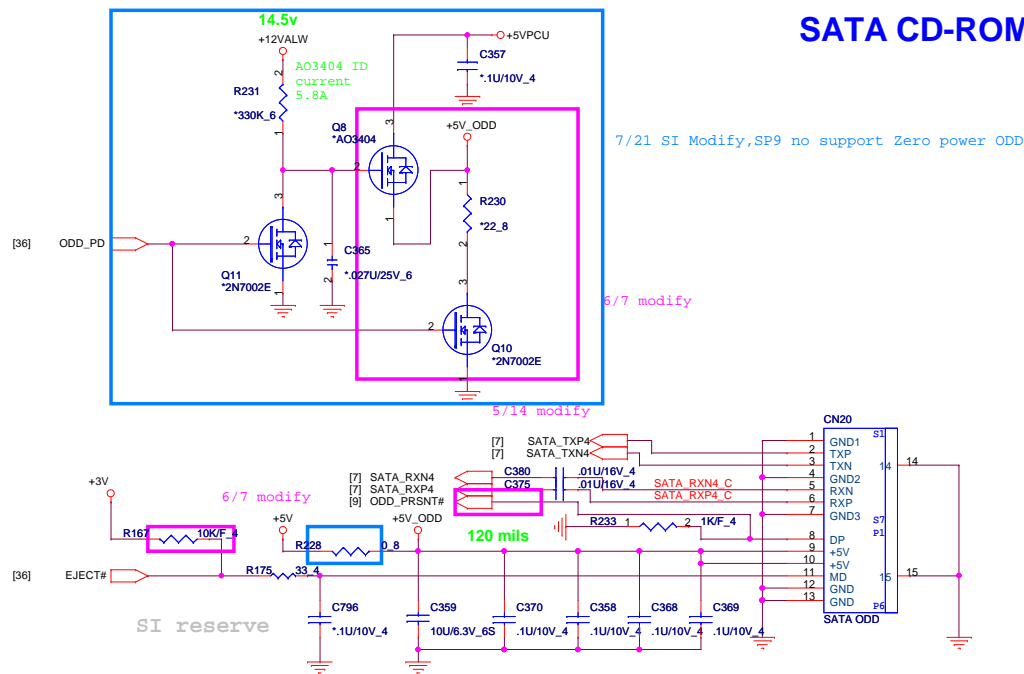
SI change type

+3V [2,6,7,8,9,10,12,13,14,17,24,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47]
+5V_AVDD [29,30]
+VIN [25,39,40,41,42,43,44,45,46,48]



SATA CD-ROM

E-SATA

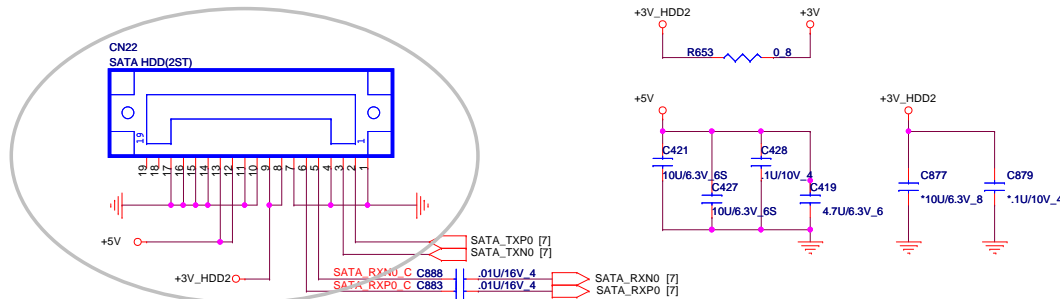


SATA HDD #1

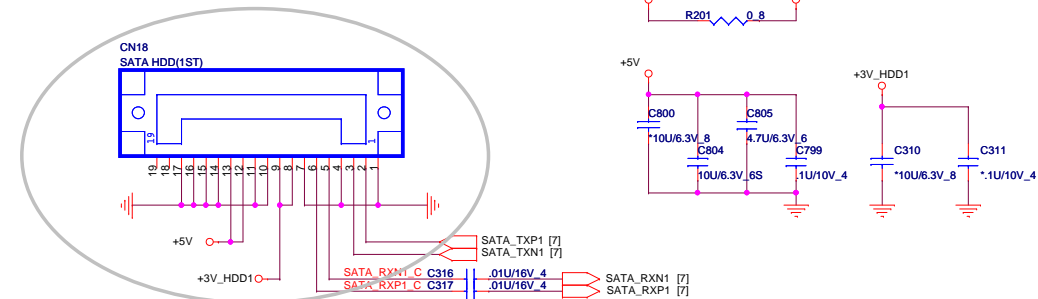
SATA HDD #2

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SI change pin define and footprint (the same AX)

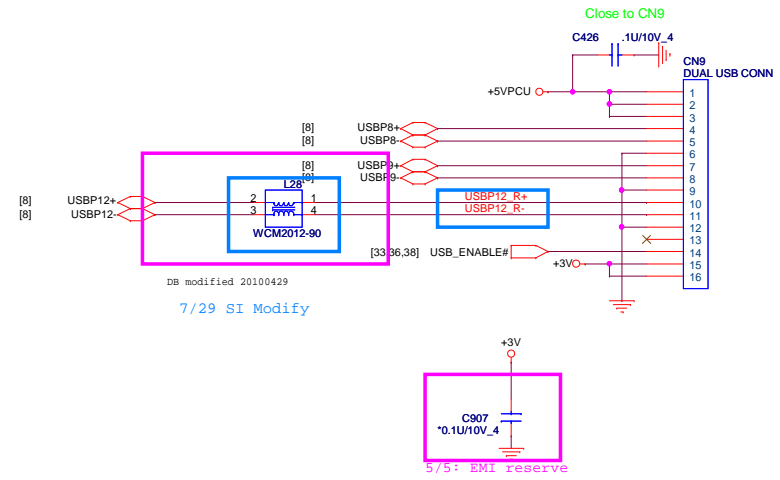
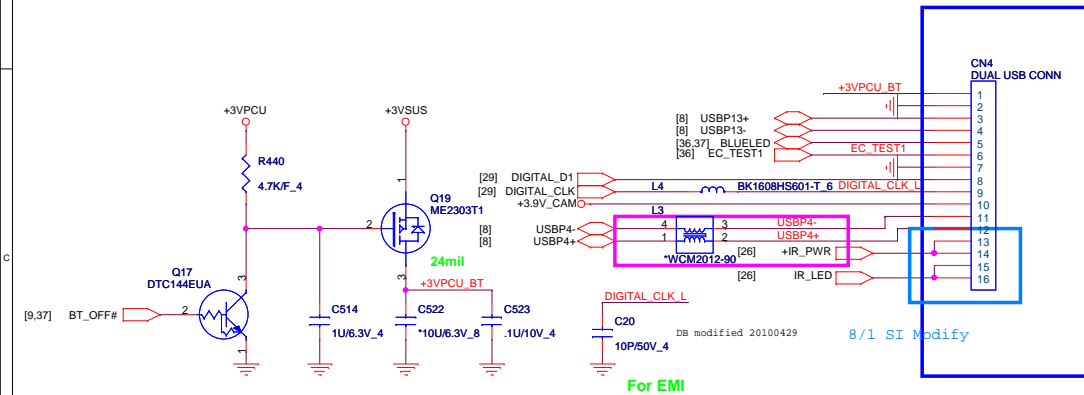


SI change pin define and footprint (the same AX)



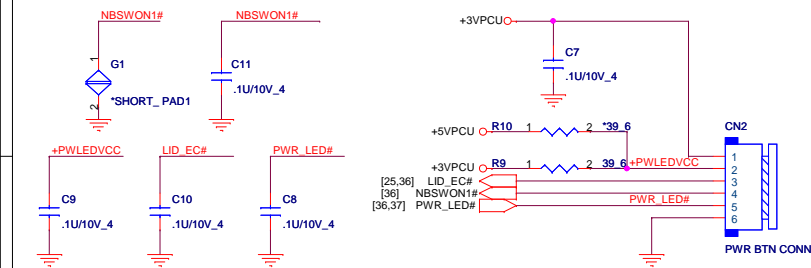
Bluetooth

Ext USB & Card Reader

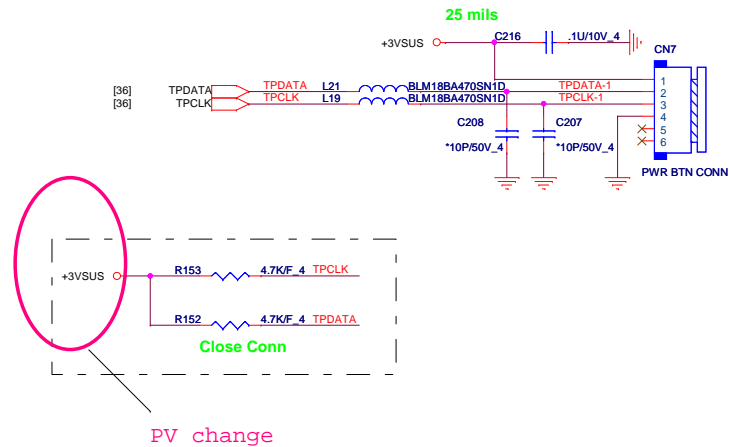


Power Button Touch Pad Button

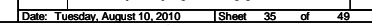
www.aitech1.ru

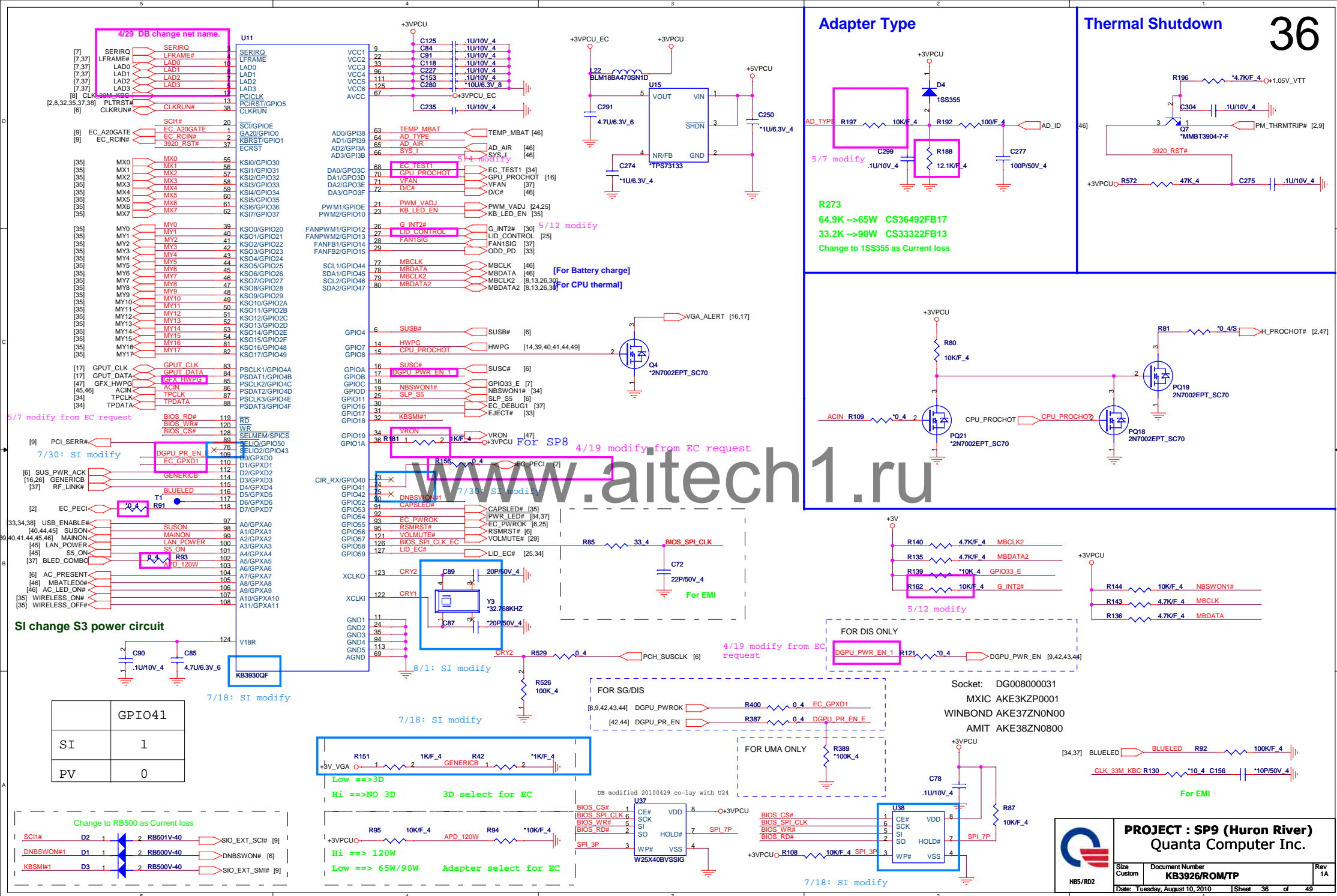


1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND



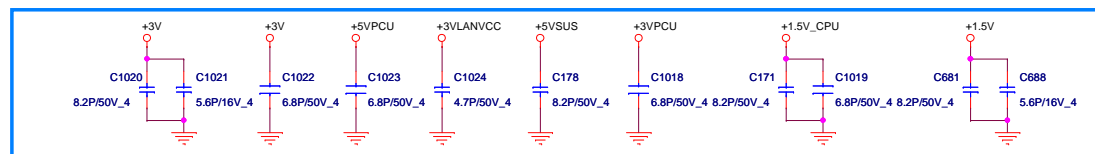
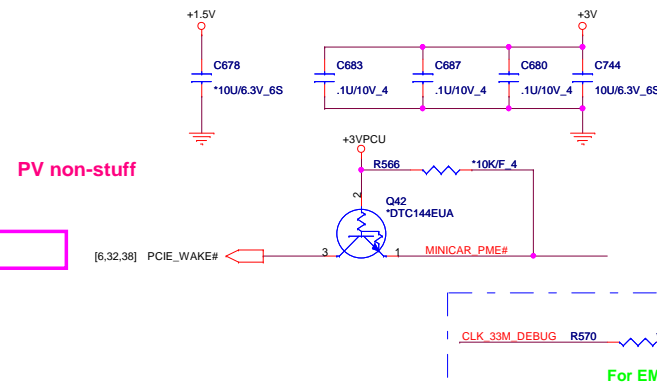
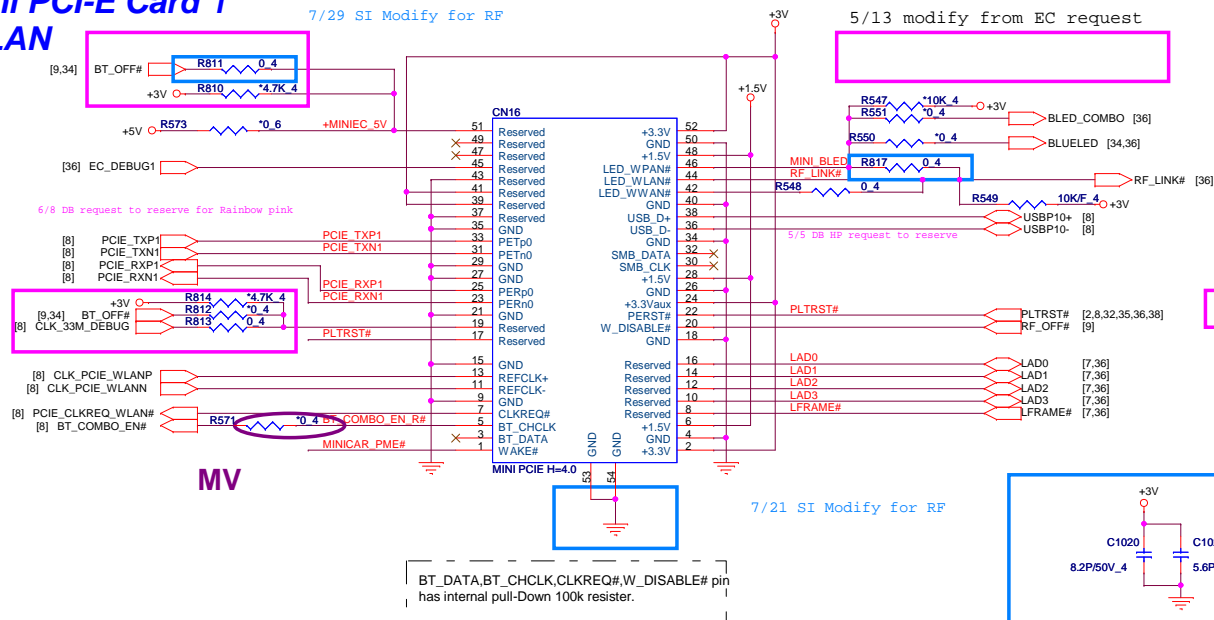
35



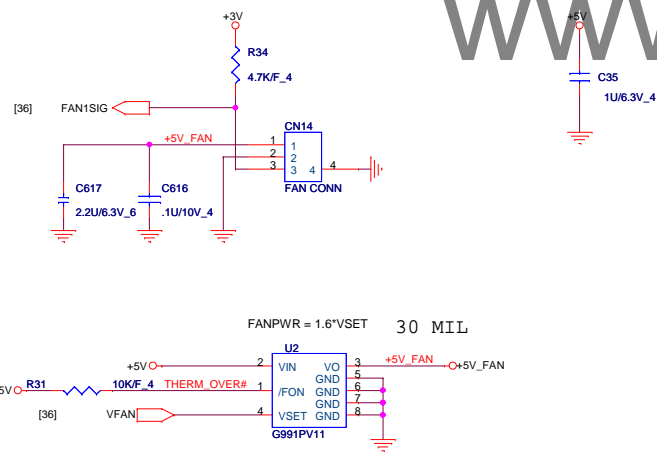


Mini PCI-E Card 1

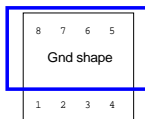
7/29 SI Modify for RF



CPU FAN



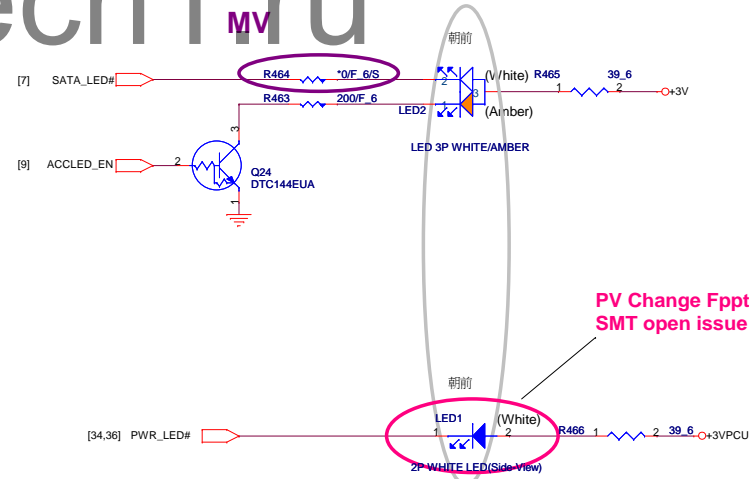
G995 layout notice



LED

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SI Change Fpptprint



PV Change Fpptprint for solve SMT open issue

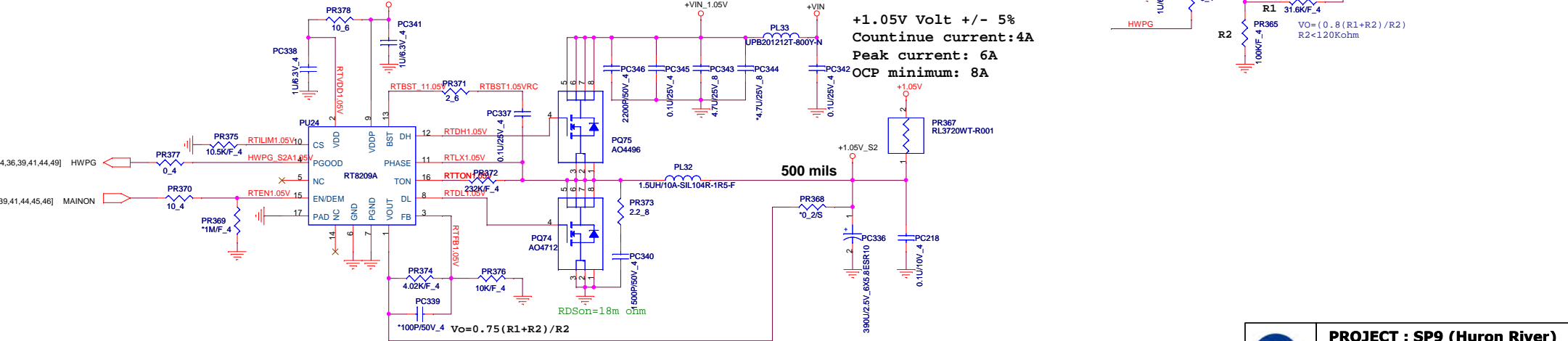


PROJECT : SP9 (Huron River)
Quanta Computer Inc.

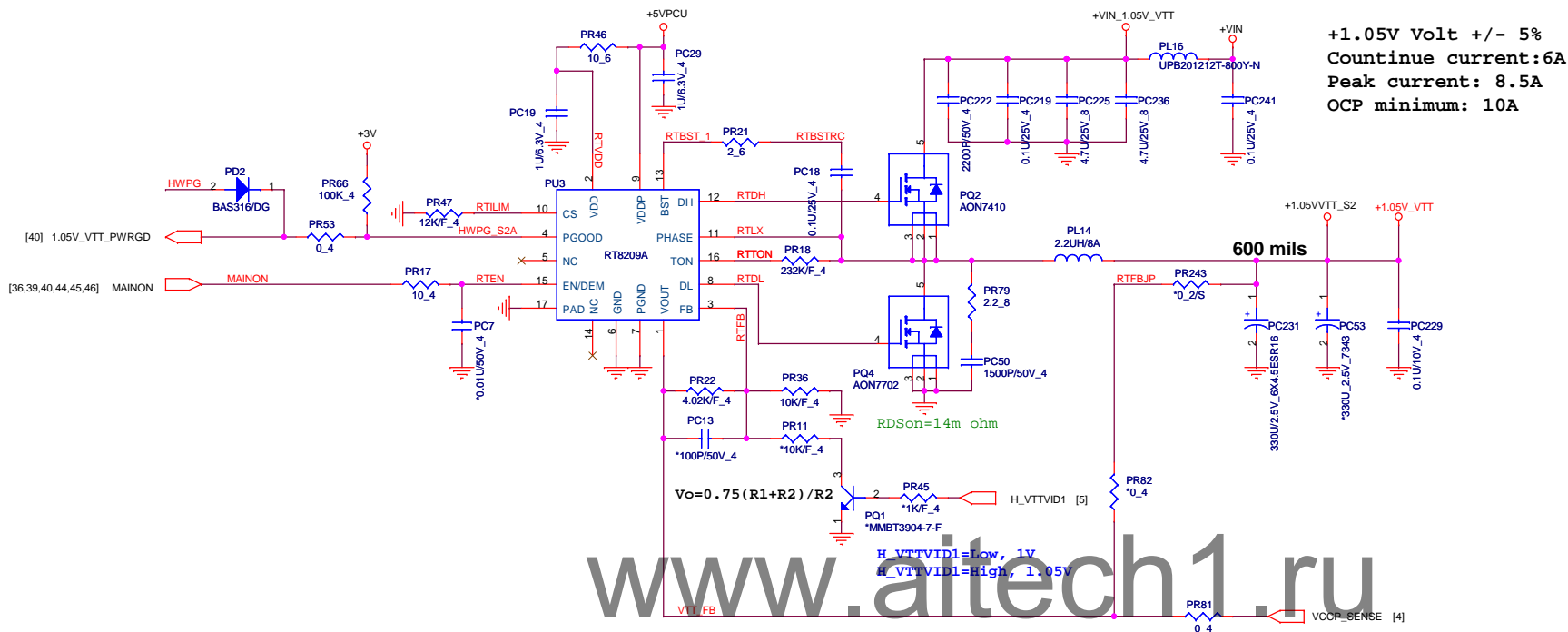
Size Custom	Document Number MINI PCIE CONN X2	Rev 1A
Date: Tuesday, August 10, 2010		Sheet 37 of 49



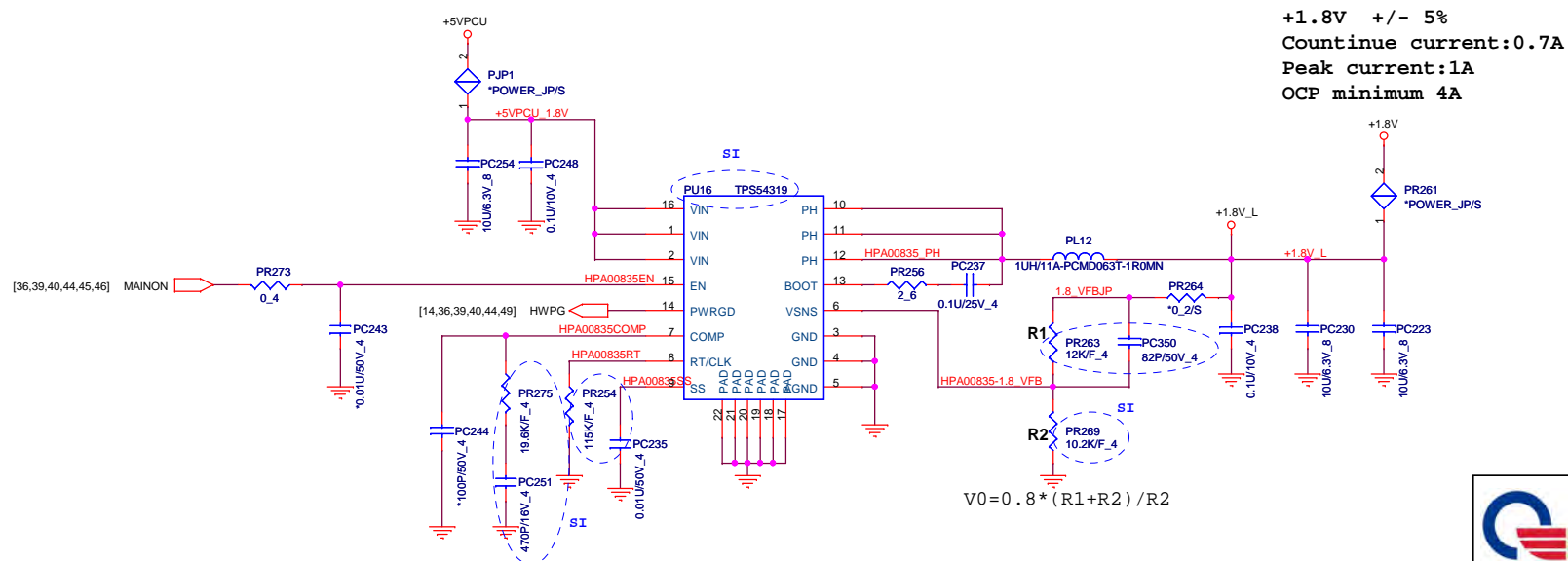
Clock select signal	
USB3.0_CSEL	High = External 48Mhz
	Low = 24MHz X'tal



	VCCSA_SEL	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.8V
1	1	0.8V

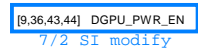


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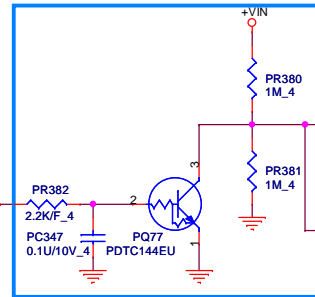


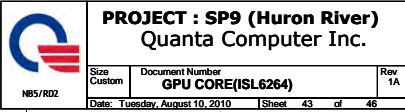
PROJECT : SP9 (Huron River)
Quanta Computer Inc.

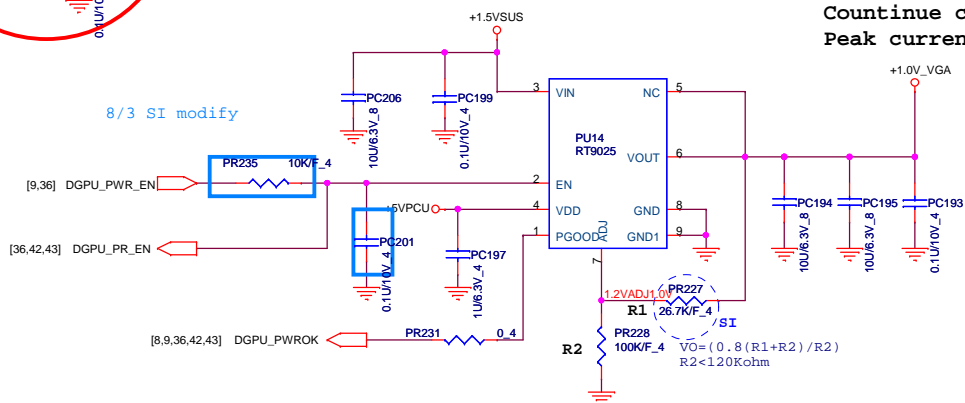
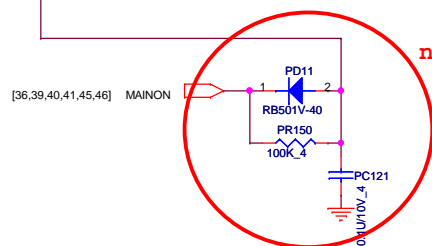
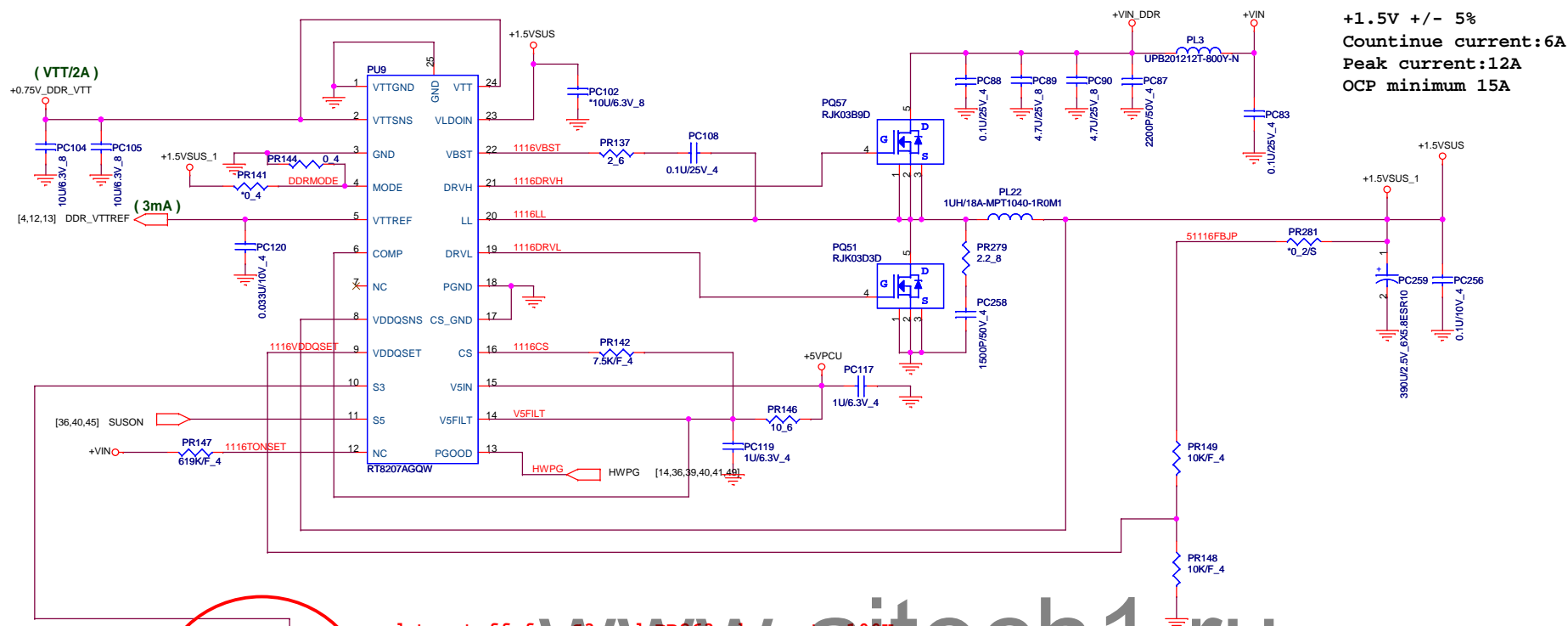
Size Custom	Document Number +1.05V/+1.8V (RT8204C)	Rev 1A
Date: Tuesday, August 10, 2010	Sheet 41	of 46



7/2 SI modify

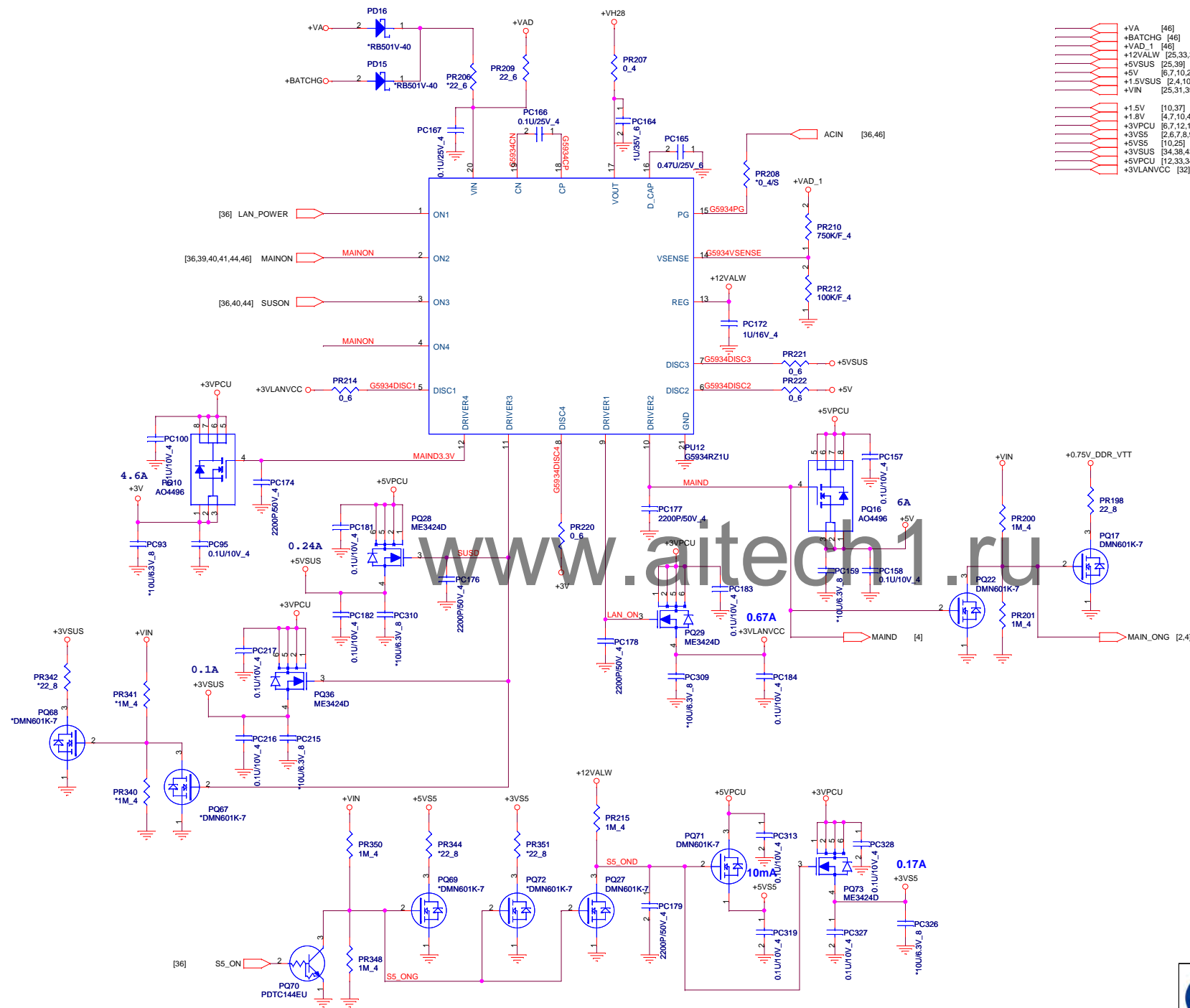






PROJECT : SP9 (Huron River)
Quantia Computer Inc.

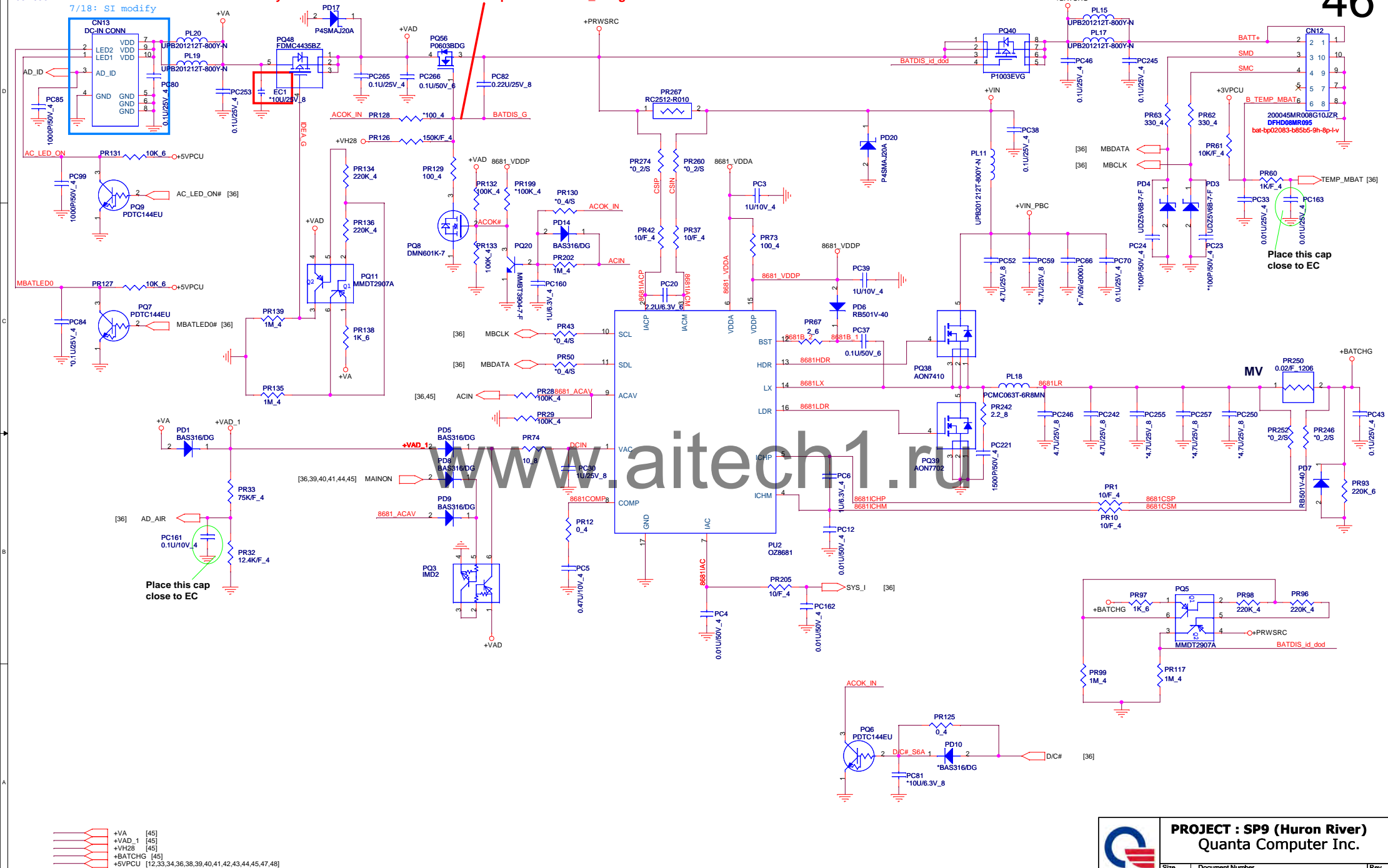
Size Custom	Document Number DDR3 (RT8207)	Rev 1A
Date: Tuesday, August 10, 2010 Sheet 44 of 46		



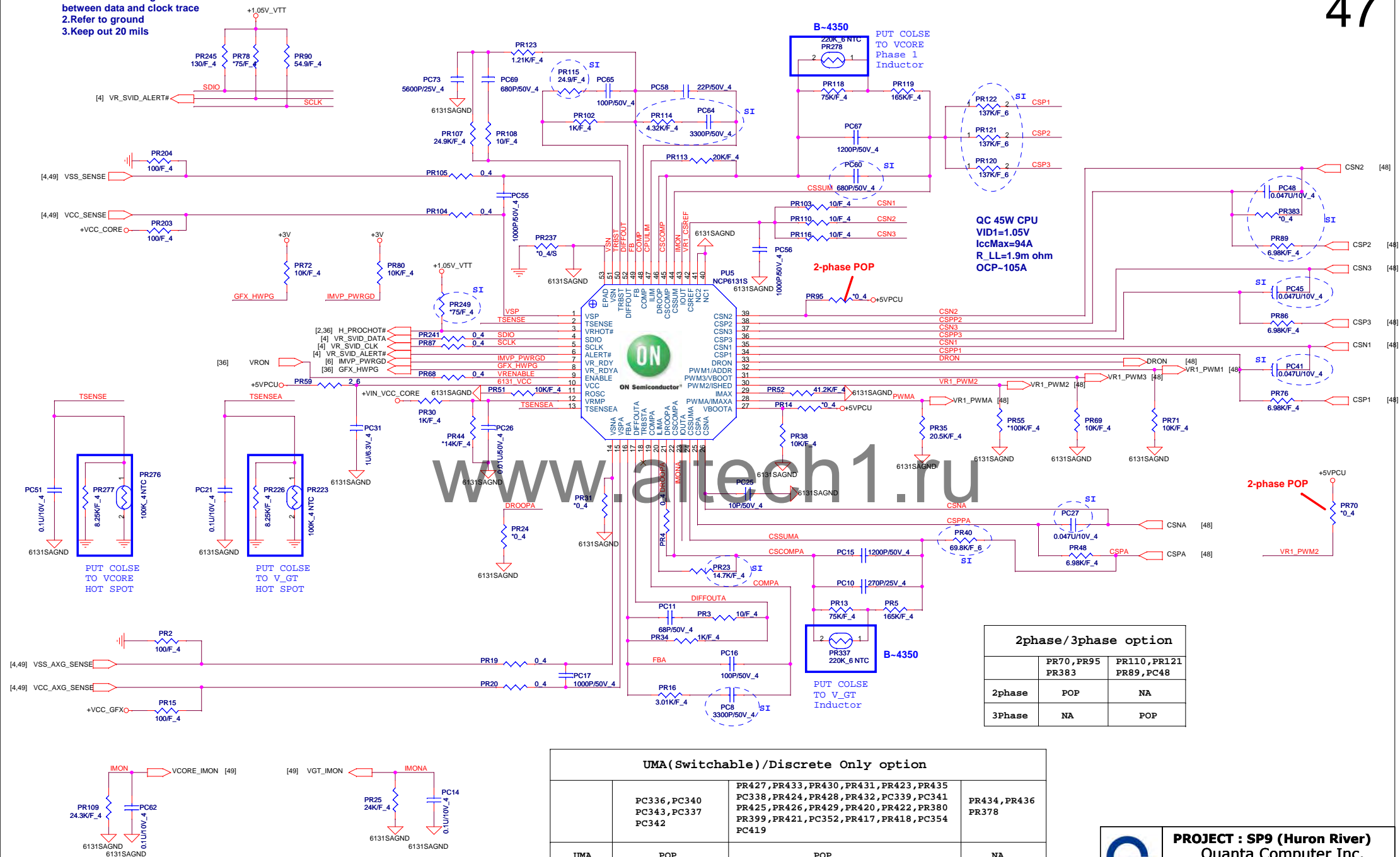
TOP DC_JACK
65W/90W

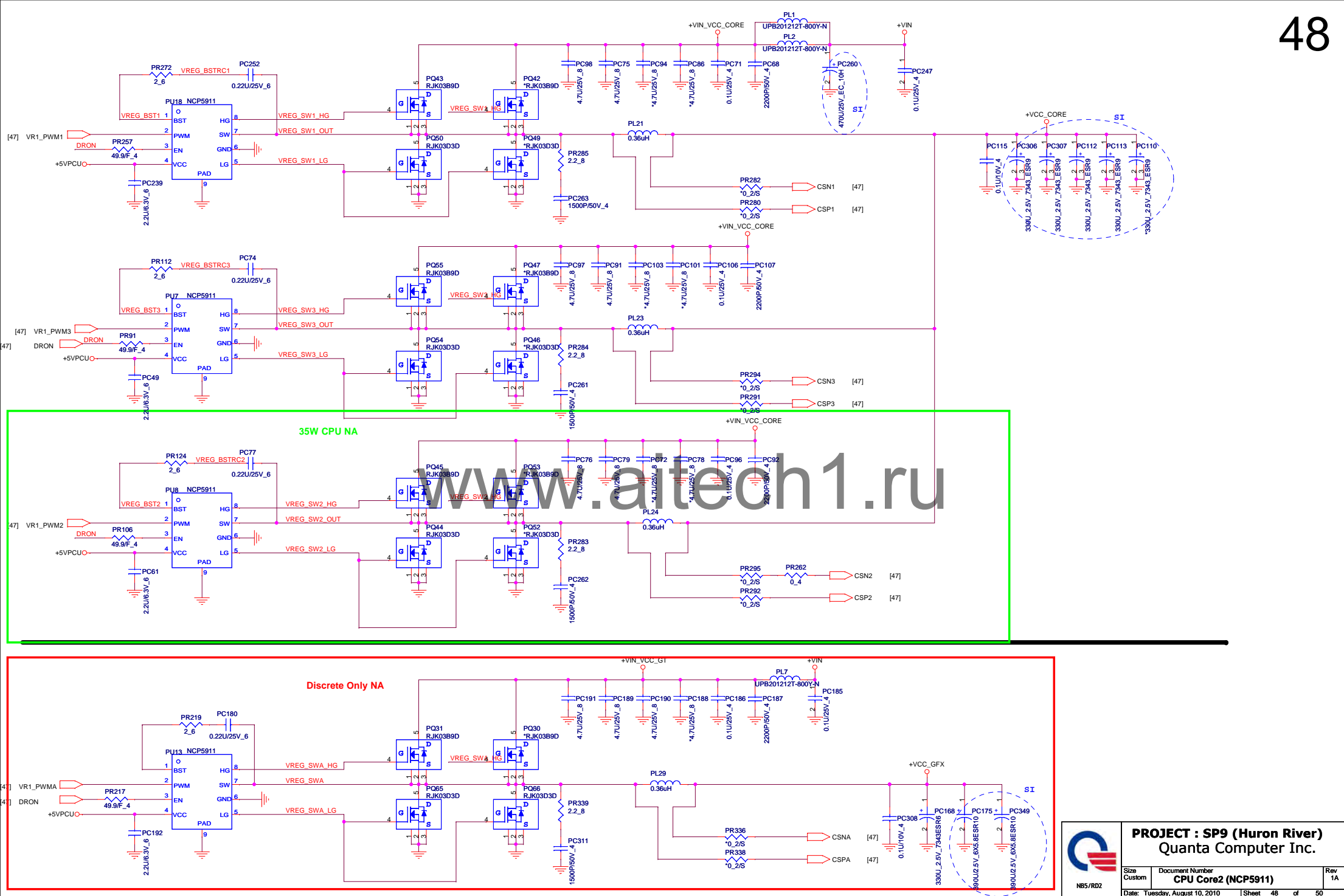
For EMI test only no stuff

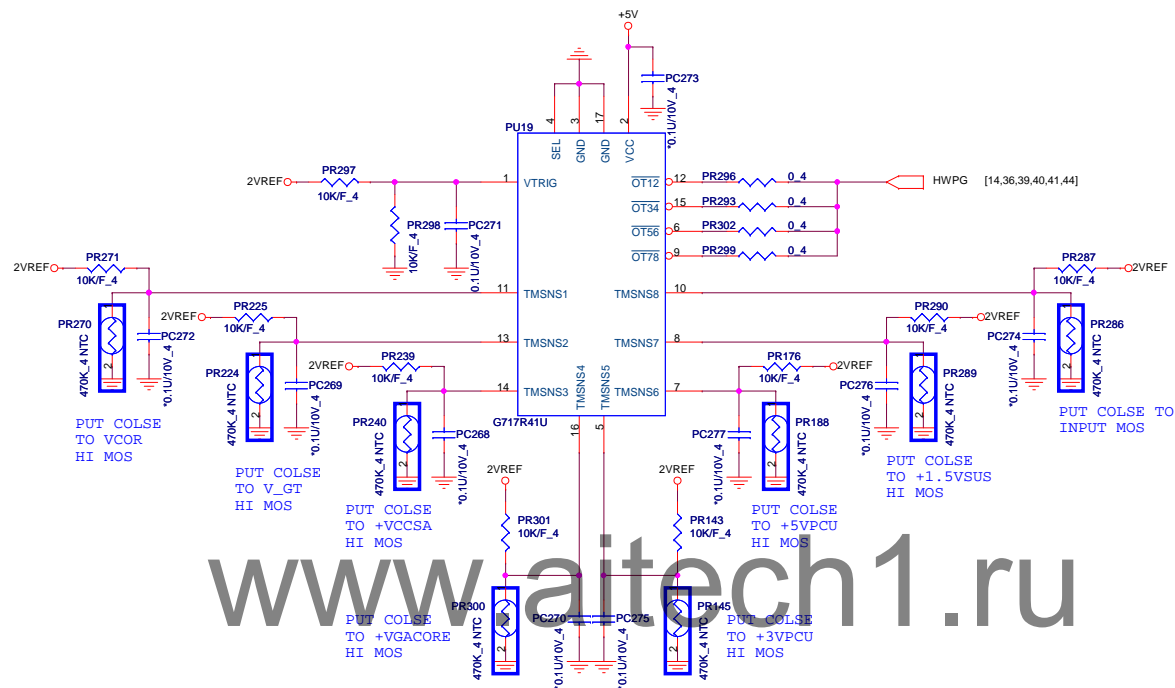
Do Not add test pad on BATDIS_G signal



- 1.Alert trace routing between data and clock trace
- 2.Refer to ground
- 3.Keep out 20 mils







Vender	Size	P/N
EON	128KB	
	512KB	AKE37ZN0Q01 (EN25F40-100HIP)
Winbond	128KB	AKE35FN0N00 (W25X10BVSNIG)
	512KB	AKE37FN0N01 (W25X40BVSSIG)
Socket		DG008000031